Theory, Modelling and Implementation of Graphene Field-Effect Transistor

by

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TO MY FAMILY

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Abstract

Two-dimensional materials with atomic thickness have attracted a lot of attention from researchers worldwide due to their excellent electronic and optical properties. As the silicon technology is approaching its limit, graphene with ultrahigh carrier mobility and ultralow resistivity shows the potential as channel material for novel high speed transistor beyond silicon.

This thesis summarises my Ph.D. work including the theory and modelling of graphene field-effect transistors (GFETs) as well as their potential RF applications. The introduction and review of existing graphene transistors are presented. Multiscale modelling approaches for graphene devices are also introduced. A novel analytical GFET model based on the drift-diffusion transport theory is then developed for RF/microwave circuit analysis. Since the electrons and holes have different mobility variations against the channel potential in graphene, the ambipolar GFET cannot be modelled with constant carrier mobility. A new carrier mobility function, which enables the accurate modelling of the ambipolar property of GFET, is hence developed for this purpose. The new model takes into account the carrier mobility variation against the bias voltage as well as the mobility difference between electrons and holes. It is proved to be more accurate for the DC current calculation. The model has been written in Verilog-A language and can be import into commercial software such as Keysight ADS for circuit simulation.

In addition, based on the proposed model two GFET non-Foster circuits (NFCs) are conducted. As a negative impedance element, NFCs find their applications in impedance matching of electrically small antennas and bandwidth improvement of metasurfaces. One of the NFCs studied in this thesis is based on the Linvill's technique in which a pair of identical GFETs is used while the other circuit utilises the negative resistance of a single GFET. The stability analysis of NFCs is also presented. Finally, a high impedance

surface loaded with proposed NFCs is also studied, demonstrating significant bandwidth enhancement.

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Table of Contents

List of Figures

List of Tables

List of Abbreviations

2D	Two-Dimensional
h-BN	Hexagonal Boron Nitride
TMD	Transition Metal Dichalcogenide
BP	Black Phosphorous
CVD	Chemical Vapour Deposition
FET	Field-Effect Transistor
DoS	Density of State
GFET	Graphene FET
NFC	Non-Foster Circuit
BJT	Bipolar Junction Transistor
Op-amp	Operational Amplifier
RTD	Resonant Tunnelling Diode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RF	Radio-Frequency
GNR	Graphene Nanoribbon
GO	Graphite Oxide
rGO	Reduced Graphene Oxide
GIC	Graphite Intercalation Compounds
NMP	Nmethylpyrrolidone
UHV	Ultra-High Vacuum

C_2H_4	Ethylene
C_2H_2	Acetylene
PMMA	Polymethyl Methacrylate
Ge	Germanium
FoM	Figures of Merit
CS	Common-Source
CD	Common-Drain
CG	Common-Gate
pHEMT	Pseudomorphic High-Electron-Mobility Transistors
HEMT	High-Electron-Mobility Transistors
mHEMT	Metamorphic High-Electron-Mobility Transistors
HET	Hot-Electron Transistor
EBI	Emitter-Base Insulator
BCI	Base-Collector Insulator
NEGF	Nonequilibrium Greens Function
2DEG	Two-Dimensional Electron Gas
LO	Local Oscillator
IF	Intermediate Frequency
IIP3	Input Third-order Intercept Point
PSK	Phase Shift Keying
FSK	Frequency Shift Key
EOT	Equivalent Oxide Thickness
ESA	Electrically Small Antenna
PCB	Printed Circuit Board
OCS	Open Circuit Stable
SCS	Short Circuit Stable
EM	Electromagnetic
RHP	Right-Half Plane

LHP   Left-Half Plane

W/L   Width-to-Length Ratio

HIS   High Impedance Surface

PEC   Perfect Electric Conductor

Chapter 1

Introduction

The emerging two-dimensional (2D) materials with atomic thickness have been of great interest to scientists and engineers in the last decade. At the moment, the most-explored 2D materials are graphene, hexagonal boron nitride (h-BN), transition metal dichalcogenides (TMDs), black phosphorous (BP), etc. As the first isolated 2D material [1], graphene has been produced through mechanical exfoliation, chemical vapour deposition (CVD) and other approaches like epitaxial growth on SiC substrate. Due to the extraordinary electronic, thermal, optical and mechanical properties, 2D materials have been considered as potential candidates for the development of novel electronic and optoelectronic devices. Their excellent scalability also enables further miniaturisation of electronic components for the future generation of semiconductor technology.

1.1 Graphene and Two-dimensional Materials

Graphene, sometimes also considered as unzipped carbon nanotube (Fig. 1.1), is a gapless material with a measured record of carrier mobility exceeding 1,000,000 cm^2/V $\cdot$ s in suspended form at 4 K [2]. As we know. the carrier mobility (μ) describes how fast electron or hole moves under certain electron field (E): $v_d = \mu E$, where v_d is the drift

<center>(a)</center>

<center>(b)</center>
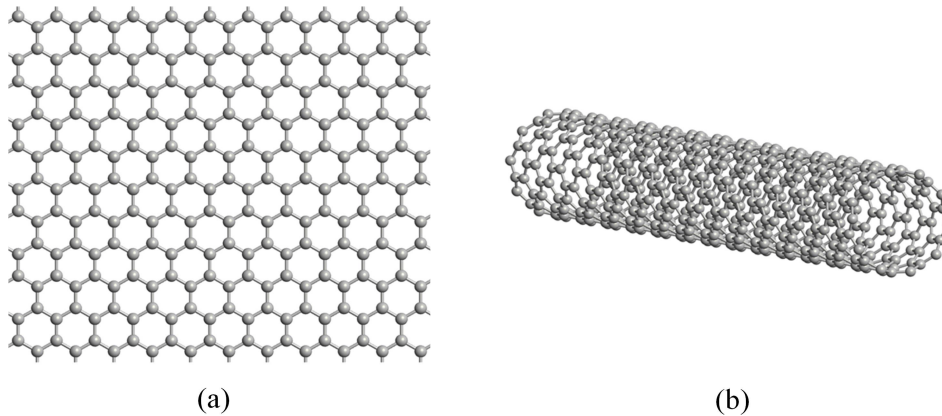
Figure 1.1: Atomic structure of (a) graphene (b) single-walled carbon nan-
otube

velocity that illustrates the average velocity a carrier can reach under E. This ultra
high mobility of graphene, beyond any known semiconducting materials, is of particular
interest for the development of novel high-speed devices. It is shown in Fig. 1.2 (a)
that the number of publications on graphene has been increasing exponentially during
the last decade. Graphene has been used to develop field-effect transistors (FETs) [3–
5]. The ambipolar conducting property of graphene allows either electron or hole as
the major carriers. By applying a gate voltage perpendicular to the graphene channel,
the electrostatic doping of graphene is realized and the channel resistance varies as a
function of gate voltage. Unfortunately, due to the nature of zero gap between valence
and conduction band of graphene, the on/off current ratio of graphene FET (GFET) is
significantly smaller than the requirement of digital circuits [6]. Therefore, the potential
application of GFET is focused on analog/RF circuits. It has been predicted in [7] that
thanks to the ultrahigh carrier mobility of graphene, the intrinsic cut-off frequency of
sub-10 nm GFET is in the range of THz regime, making it attractive for high frequency
applications. However, when graphene is deposited onto substrate like SiO_2, its mobil-
ity is significantly degraded compared with the suspended case [1, 8]. This is because
of the impurity scattering induced by the charged impurities in the SiO_2 substrate[9].
Meanwhile, the negative differential resistance (NDR) of GFET has also been reported,
providing an alternative option for devices in analog/RF applications [10].
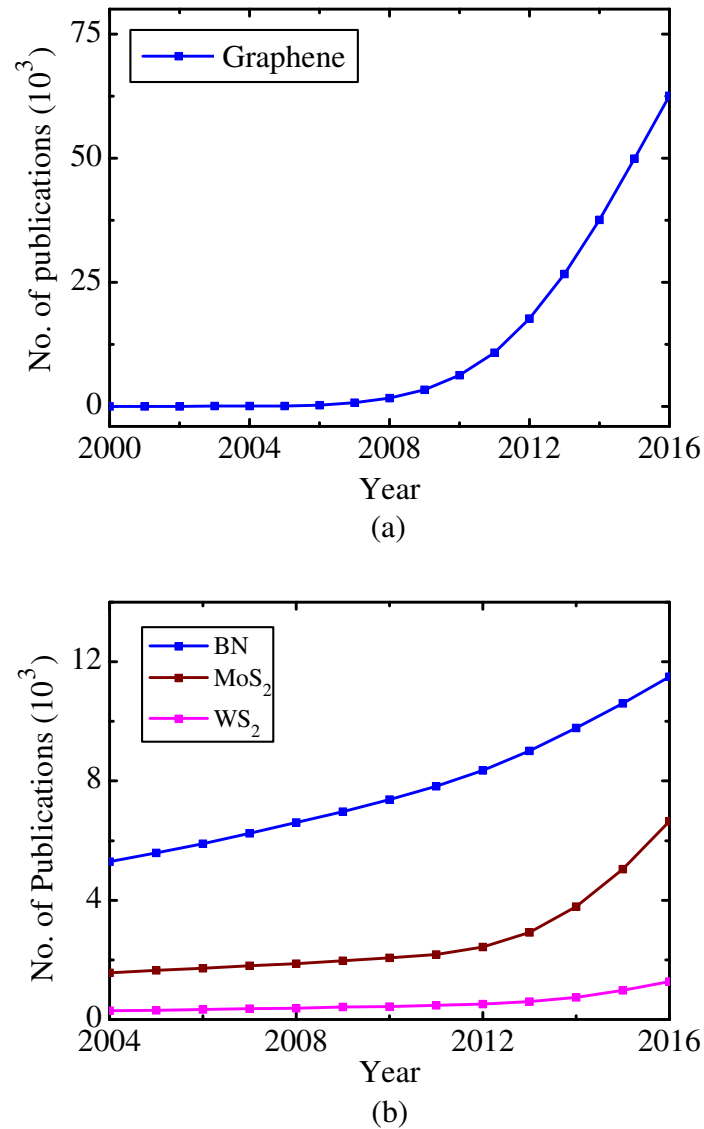
Figure 1.2: Number of publications on (a) graphene and (b) BN, MoS_2 and WS_2. Sourced from Web of Science.

In 2007, a theoretical calculation predicted the generation of a bandgap for graphene on h-BN substrate [11], resulting in a significant increase in the exploration of h-BN. From Fig. 1.2(b) one can see the number of publications on h-BN has been doubled in the last 10 years. h-BN also has hexagonal lattice structure, as shown in Fig. 1.3(a). Although it was revealed later that as a insulator h-BN could not open a bandgap in graphene, it turned out to be a perfect substrate to preserve graphene's ultrahigh carrier mobility [12] due to the reduced charged impurities (compared with grahene-on-SiO_2)
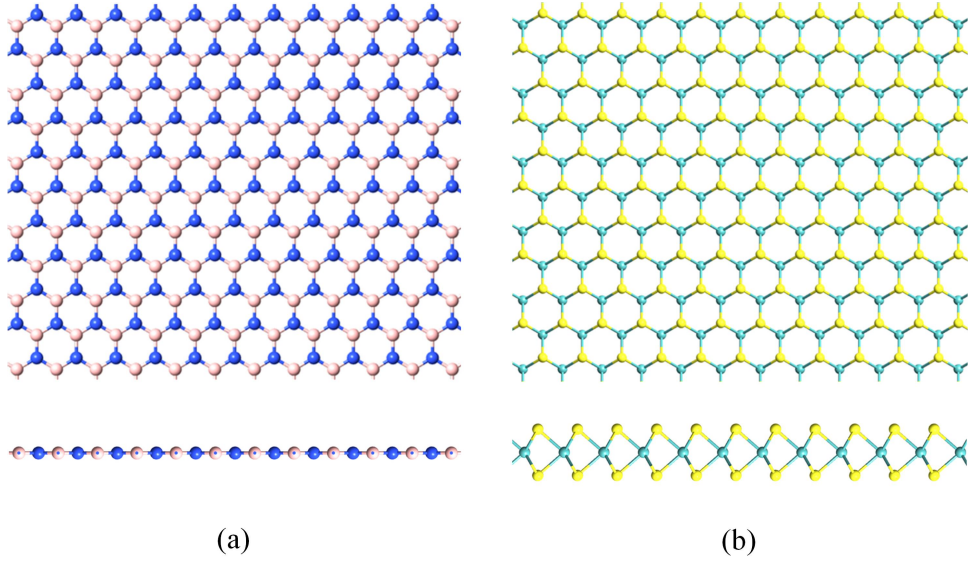
Figure 1.3: Atomic structure of (a) h-BN (b) MoS_2.

[12]. However, the mobility of graphene-on-h-BN is still lower than that of suspended graphene.

Soon after the discovery of graphene, other 2D materials like TMDs (e.g. MoS_2, WS_2) were also prepared through mechanical exfoliation [13, 14] or CVD method [14, 15]. Among them, MoS_2 is the most well-explored material with the hexagonal lattice structure (trigonal prismatic (2H) phase) shown in Fig. 1.3(b). Intersetingly, the bandstructure of TMDs changes while the thickness is reduced from bulk to monolayer. For instance, monolayer MoS_2 has a large direct bandgap of 1.95 eV while bulk MoS_2 exhibits a indirect bandgap of 1.2 eV [16]. Experimental results have shown that the wide bandgap of monolayer MoS_2 can prevent MoS_2 FETs from short-channel effects [17–19]. However, the measured carrier mobility in monolayer MoS_2 on SiO_2 substrate is only up to a few hundred $cm^2/V \cdot s$ due to the optical photon scattering [20–22], limiting their applications in high frequencies. Meanwhile, FETs based on other TMDs also suffer from the relatively low carrier mobility [23–26].

Black phosphorus (BP) is another emerging 2D material with atomic thickness. Monolayer BP is also known as phosphorene. It is a semiconductor with 0.3 eV indirect

bandgap in bulk form and 1.8 eV direct bandgap when the thickness is decreased to the monolayer limit [27, 28]. Thanks to the narrow bandgap of few-layer BP, it is able to absorb light from visible to near-infrared regime efficiently, enabling the development of BP-based photodetectors [29–31]. The room-temperature hole mobility over 5000 $cm^2/V \cdot s$ has been predicted for BP while the calculated electron mobility of few-layer BP is significantly lower (1000 $cm^2/V \cdot s$) [32–34]. The measured hole mobility in BP FETs varies from a few hundred to 1000 $cm^2/V \cdot s$. The h-BN sandwiched BP has also been reported, demonstrating an improved hole mobility of 1350 $cm^2/V \cdot s$ [35]. The implementation of h-BN also helps to improve the device stability under ambient condition as BP would easily react with the oxygen in air [36], which can significantly degrade the device performance.

1.2 Non-Foster Circuit

Foster's reactance theorem [37] reveals that the reactance of a two-terminal passive lossless device (e.g. capacitor and inductor) should increase monotonically with frequency, as show in Fig. 1.4(a). The non-Foster circuit (NFC), in contrast, is an active device whose reactance decreases monotonically with frequency. Compared with the passive matching that only achieves zero reactance at a pre-designed resonant frequency (Fig. 1.4(a)), the realisation of NFCs enables the active impedance matching over a broad frequency range, as shown in Fig. 1.4(b). So far, NFCs have been realised with Linvill's approach utilising a pair of bipolar junction transistors (BJTs) [38]. Other methods using operational amplifier (Op-amp) or resonant tunnelling diode (RTD) have also been reported [39, 40]. The implementations of NFC include active impedance matching of electrically small antenna and bandwidth extension of metasurface structures such as high impedance surface (HIS).
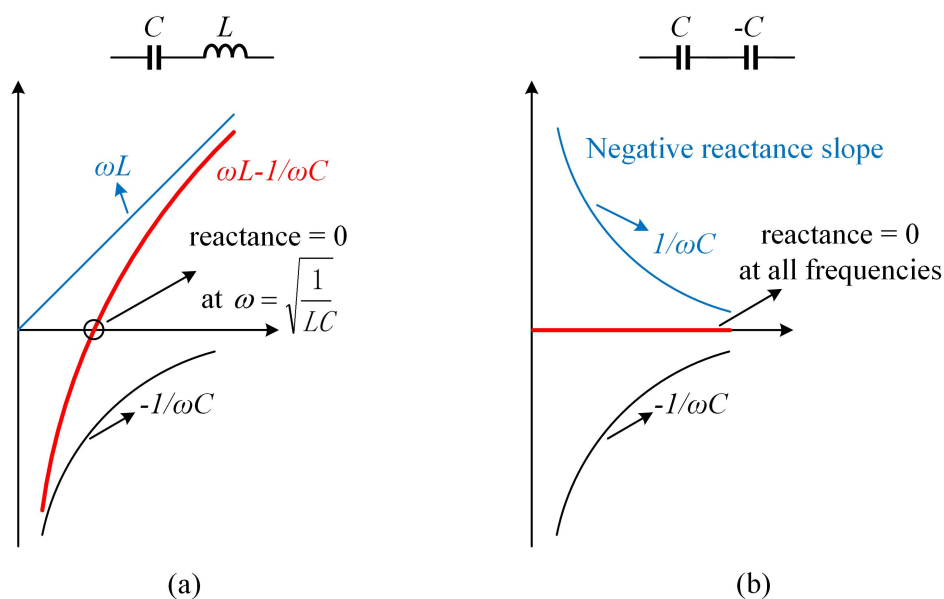
Figure 1.4: Impedance matching techniques (a) passive and (b) active.

1.2.1 History of Non-Foster Circuit

The negative resistance of vacuum tubes was observed by Albert Hull at General Electric in 1918 [41]. About two years later, the concept of NFC, also known as negative impedance converter (NIC), demonstrating negative capacitance or inductance, were proposed by Marius Latour [42]. In 1931, George Crisson et al. at Bell Labs successfully developed a negative resistance as telephone line repeaters with vacuum tubes [43]. Two decades later, the vacuum tube based NFCs were also presented by Merrill [44]. However, it was not until 1953, when the first NFC based on BJTs was demonstrated by Linvill [38], that NFC became of great interest to the engineers. The approach of Linvill's NFC belongs to the voltage-inversion technology. Later in 1957, Larky and Yanagisawa presented their BJT-based current-inversion NFCs individually [45, 46]. Today, the novel BJT NFCs utilizing surface mounted components have successfully demonstrated negative impedance at microwave frequencies. In addition to BJTs, the operational amplifiers (Op-amps) were also used to achieve negative impedance [39, 47, 48]. The Op-amp NFCs have simpler circuit schematic and are easier to stabilise compared with the BJT-based counterparts. This is because it is convenient to define the poles and zeros of the Op-amp

with external components. However, Op-amp NFCs suffer from low operation frequency and small bandwidth due to the fixed gain-bandwidth product of Op-amps and the associated parasitics [49]. Recently, the fully-integrated broadband negative inductances, operating in gigahertz regime have also been developed using CMOS or BICOMS process [50–52]. These circuits are all based on Linvill's model or the modified version. Due to the complexity of Linvill's circuit, the simplified NFCs based on negative resistance of tunnel diode and resonant tunnelling diode (RTD) have been explored in Ref. [53, 54]. The idea of converting negative resistance to negative impedance can be tracked back to the 1920s [55–57]. With only one active device and less biasing components, the dimension of negative-resistance-based NFC has been significantly reduced.

1.3 Research Objectives

The main objectives of this study are presented as below:

1. Derive an accurate closed-form analytical model for GFET. The existing GFET models either need to be solved numerically or exhibit poor accuracy in modelling the ambipolar transfer characteristic of GFET. In this thesis, an accurate GFET model will be developed for circuit analysis. The model should have an analytical form and is compatible with Spice or Verilog-A language.

2. Explore the implementation of GFET for NFC design. In this case, we focus on the design of Linvill's NFC model with a pair of cross-coupled GFETs. Due to the ultrahigh carrier mobility of graphene, GFETs are predicted to exhibit higher cutoff frequency than other existing transistors. Hence, it would be interesting to investigate the potential of GFET-based NFC for high frequency applications.

3. Explore the realization of NFC utilizing the NDR behaviour of GFET. The NFC based on the NDR of RTD has been demonstrated. The RTD-based NFC has much simpler circuit layout compared with the Linvill's model and can potentially

operate at higher frequency with miniaturized physical dimensions. As GFET also shows NDR effect, it provides us an alternative way to achieve high-performance NFC based on the graphene platform.

4. Demonstrate the implementation of Graphene NFC for bandwidth improvement of HIS. The passive HIS exhibits a narrow bandwidth near its center operation frequency. Due to its inherent limitation of passive resonance, it is impractical to achieve broadband HIS without compromising other performances such as the device thickness, loss and design complexity. Thus, the graphene NFCs are proposed as active loads to cancel the reactance of HIS and extend its operation bandwidth.

1.4 Thesis Outline

This thesis is organised as follows:

Chapter 1 depicts the goals of research as well as the organisation of this thesis. A short introduction of 2D materials and NFC is also included.

Chapter 2 presents a review on electronic and optical properties of graphene. Several approaches used in graphene synthesis are introduced. Graphene transistors as well as classical figures of merit for the analysis of transistor performance are also reviewed.

Chapter 3 is dedicated on the modelling of graphene transistors. The concept of multi-scale modelling for graphene transistors is illustrated and a closed-form analytical model based on the drift-diffusion transport theory is derived. The model is written into Verilog-A language that are suitable for circuit simulation with commercial software such as Keysight ADS. Finally, model validation with measurement results is also presented.

Chapter 4 explores the implementation of GFETs for NFC design. The measurement results of GFET are extracted and reproduced with the proposed model for circuit analysis. Simulation results of a Linvill's NFC utilizing a pair of cross-coupled GFETs and

a NFC based on the NDR of GFET are presented.

Chapter 5 examines the bandwidth extension of HIS utilising graphene NFCs. With simulation results presented in Chapter 4, the bandwidth extension of HIS is demonstrated and the stability analysis of actively-loaded HIS is also illustrated.

Chapter 6 concludes the thesis. Some ideas for further research are proposed as well.

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Chapter 2

Research on Graphene and Graphene Transistors

Graphene, the material once believed not existing in an isolated state, has attracted a lot of attention since it was first "peeled off" from graphite by Andre Geim and Kostya Novoselov at the University of Manchester [1]. As a single-atomic-thick 2D thin film, graphene's superior properties such as high carrier mobility, high thermal conductivity and the ambipolar transfer characteristic make it attractive for electronic applications. As predicted in Moore's low, the number of transistors in an digital integrated circuit doubles approximately every two years, leading to an annual 25% reduction in the cost of a transistor on the chip [2]. Behind this great success is the continuous scaling of silicon metal-oxide-semiconductor field-effect transistor (MOSFET). So far, the Si MOS-FETs have been successfully mass-produced with sub-10 nm gate length. Further scaling the gate length of Si MOSFET, the parameter fluctuations in the fabrication of identical transistors, short-channel effects and dominating parasitic effects will appear and degrade the device performance. Therefore, engineers and scientists are pursuing new materials as well as innovative device concepts, looking forward to extending the life of Moore's law and ensuring the continuation of semiconductor industry. Meanwhile, in another

subset area of semiconductor electronics: radio-frequency (RF) electronics, new materials with high carrier mobilities are strongly desired for high frequency devices operating at the untapped terahertz gap (0.3-3 THz). Currently, the organic field-effect transistors exhibit low carrier mobility that are not suitable for high-frequency applications. The III-V compound semiconductor based devices have demonstrated carrier mobility exceeding 10,000 $cm^2/V \cdot s$ and are widely used for high-frequency circuit designs. In addition, the devices made of compound semiconductor like GaAs can also operate at higher temperature and provide lower thermal noise compared with the silicon-based devices. However, the high cost and complicated fabrication process have limited their application in those areas where silicon cannot be used. Hence, graphene, with CMOS-compatible process and remarkable carrier mobilities far beyond that of III-V compound semiconductors, immediately attracts the attention of researchers worldwide. Some of them believe graphene could be used for transistors beyond the scaling limit of silicon devices and hence extend the life of Moore's law.

2.1 Properties of Graphene

More than eighty years ago, 2D materials with atomic thickness were considered as thermodynamically unstable due to large thermal fluctuations that force bonded atoms to fall apart [3, 4]. Therefore, for a long time in history, the existence of 2D materials like graphene was theoretically denied. With the discovery of graphene in 2004 this theory was eventually disapproved, bringing a great deal of attention to the emerging 2D materials. Graphene is a single-atom-thick graphite layer with sp^2-hybridized carbon atoms bonded in hexagonal lattice structure as shown in Fig. 1 (a). Hanns-Peter Boehm named it by combining graphite and the suffix of alkene (i.e. -ene) for the description of monolayer graphite in 1987 [5]. As the thinnest and lightest material known so far, graphene is nearly optical transparent with high thermal conductivity. The electron mobility of graphene at room temperature is significantly higher than carbon nanotube

or monocrystalline silicon, making it a candidate for the development of next generation high speed transistor. Graphene also has the lowest room-temperature resistivity known $(1.0 \times 10^{-6} \, \Omega \cdot \text{cm})$ [6] and has been used as electrode material in solar cells [7] and touch screens [8]. In this section, the properties of graphene are briefly introduced.

2.1.1 Electronic Property

Graphene is a semiconductor with zero bandgap between its valence and conduction band. Thus, it is also known as a semi-metal. The bandstructure of graphene calculated with Mathematica is shown in Fig. 2.1. The conduction and valence bands coincide at the Dirac point, resulting in the zero bandgap. By reducing the width of graphene to nanometer scale, it is possible to introduce a bandgap in graphene nanoribbons (GNRs) due to the quantum confinement effect [9]. Generally, there are two types of GNR named zigzag and armchair GNR as shown in Fig. 2.2(a) and (b), respectively. The zigzag GNR has zero bandgap regardless of the ribbon width while the later one has width-dependent non-zero bandgap, as shown in Fig. 2.3(a) and (b), respectively. In addition, a bandgap can also be achieved by inducing a perpendicular electric field to Bernal-stacked bilayer graphene [10], as shown in Fig. 2.4. The bandgap generation of graphene is very important in the development of graphene-based devices. At room temperature, the carrier mobility of suspended graphene is mainly limited by the acoustic electron-phonon scattering [12, 13]. The intrinsic room-temperature mobility up to 200,000 $\text{cm}^2/\text{V} \cdot \text{s}$ for the electron density of $10^{11} \, \text{cm}^2$ has been predicted in [12], corresponding to a resistivity of $1.0 \times 10^{-6} \, \Omega \cdot \text{cm}$. This is lower than that of silver $(1.59 \times 10^{-6} \, \Omega \cdot \text{cm})$, which has the lowest room-temperature resistivity before the discovery of graphene. The carrier density of graphene is electrostatically tunable and the electrical conductivity, which describes the ability of graphene for current conduction, reaches a minima on the order of $4e^2/h$. Here, e is the elementary charge and h is Plancks constant.

Graphene also exhibits anomalous quantum Hall effect under strong magnetic fields
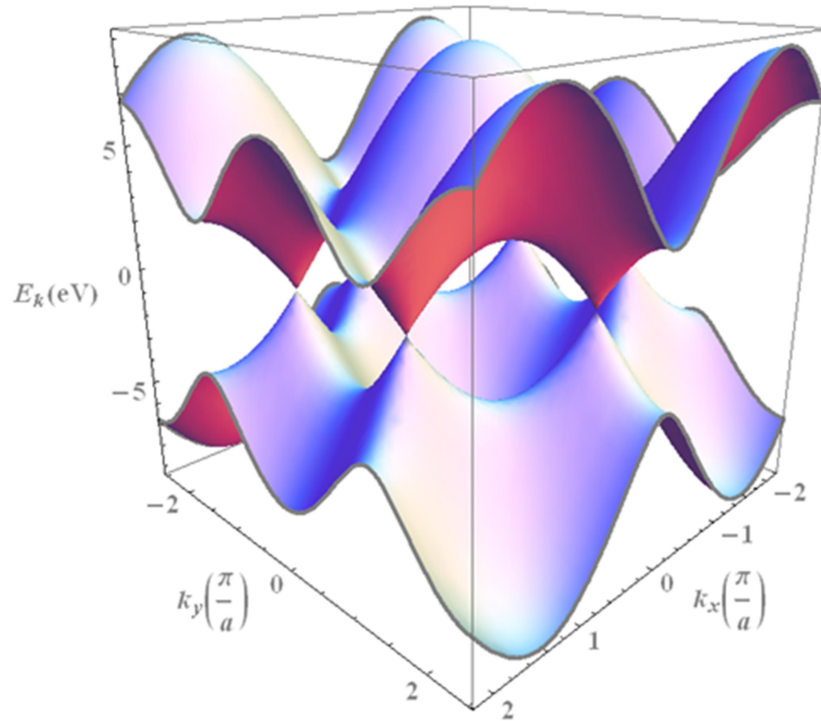
Figure 2.1: Bandstructure of graphene calculated with Mathematica.
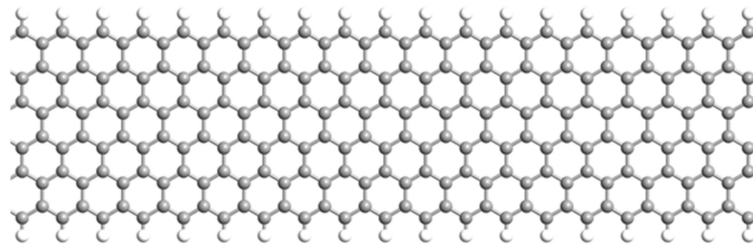
(a)
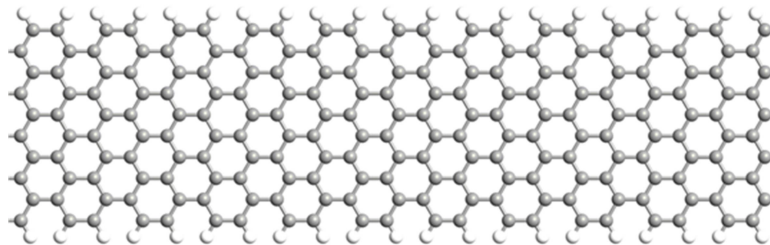
(b)

Figure 2.2: GNR with hydrogenated (a) zigzag and (b) armchair edges.
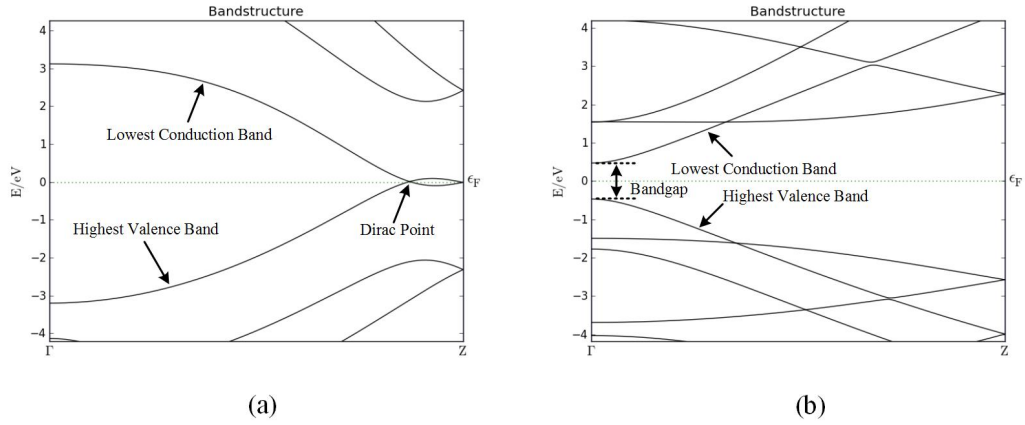
Figure 2.3: Bandstructure of GNR with (a) zigzag and (b) armchair edges. Calculated with ATK [11].
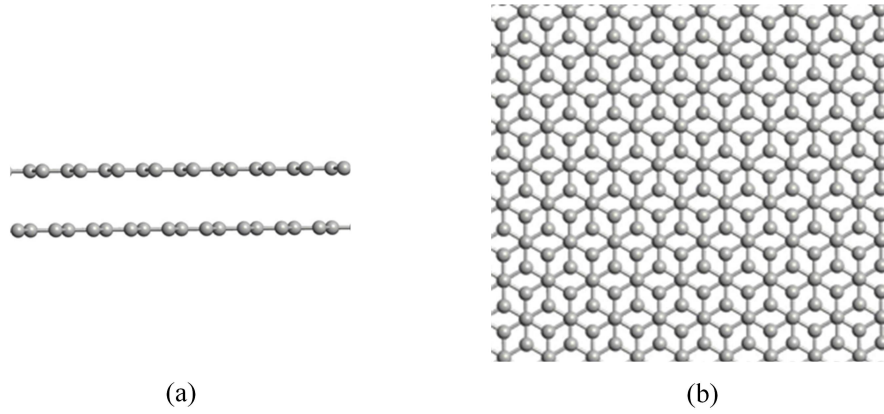
Figure 2.4: Bernal-stacked bilayer graphene (a) cross-sectional view and (b) top view.

even at the room temperature. The quantized Hall conductivity of graphene is given as

$$\sigma_{xy} = \pm 4 \left(N + \frac{1}{2} \right) \frac{e^2}{h} \tag{2.1}$$

where N is the Landau level. The coefficient 4 is because of the double valley and double spin degeneracies. It is noted that electrons and holes seem to have nearly identical mobility in suspended graphene, which is different from what has been observed in silicon [14]. When the graphene is transferred onto a SiO_2 substrate, the extrinsic surface phonon scattering introduced by SiO_2 significantly decreases its maximum achievable room-temperature mobility to 40,000 $cm^2/V \cdot s$ [12]. It has been observed that the

mobility of graphene on SiO_2 substrate decreases with the increase of temperature due to the thermal effects [12, 15, 16]. The theoretical limit of carrier mobility on SiO_2 can be approached by reducing the impurity scattering. Consequently, the mobility can further approach the intrinsic room-temperature limit (i.e. 200,000 $cm^2/V \cdot s$) by the use of alternative substrates such as h-BN [17, 18].

2.1.2 Optical Property

In the previous section, it is shown that the valence and conduction band of graphene meet each other at the Dirac point, resulting in the conical bandstructure and zero bandgap. This unique bandstructure of graphene also introduces interesting optical properties to this magic material. It has been reported that suspended graphene absorbs 2.3% optical light in vacuum [19]. As an atomic-thick material, this unexpected opacity is attributed to the unique electronic structure of graphene [20]. In addition, Graphene also exhibits saturable absorption above certain threshold optical intensity from visible to near-infrared region[21]. This saturable absorption of graphene is also observed at microwave and THz bands due to zero-bandgap-induced broadband absorption [21]. The gate-tunable photoresponse of graphene has also been experimentally demonstrated from ultraviolet to visible regime [22], indicating wideband application of graphene-based optical devices.

2.1.3 Other Properties

The bond length between carbon atoms in graphene is approximately 1.42 Å and the interlayer spacing between graphite layers is 3.35 Å [23, 24]. Although graphene is single atom thick, it is harder than diamond and its strength is 200 times that of steel. Actually graphene is the strongest material ever known, demonstrating a Youngs modulus of 1 TPa [25]. Besides, an early work also reveals that suspended graphene exhibits an extraordinary room-temperature thermal conductivity of $\sim$5300 $W \cdot m^{-1} \cdot K^{-1}$ [26]. This

is significantly higher than that of pyrolytic graphite ($\sim$2000 W$\cdot$m$^{-1} \cdot$K^{-1}) and carbon nanotube ($\sim$3500 W$\cdot$m$^{-1} \cdot$K^{-1}). Later, due to the uncertainties in the measurement and differences in the quality of graphene, [27–30] suggest the practical thermal conductivity of suspended graphene should be between 1500$\sim$2500 W$\cdot$m$^{-1} \cdot$K^{-1}. What is worse, when graphene is transferred onto a substrate, the interaction between graphene and substrate drastically reduces the phonon lifetime and suppresses the contribution of flexural phonons to the heat conduvtivity. As a result, the thermal conductivity is further reduced to 500$\sim$600 W$\cdot$m$^{-1} \cdot$K^{-1} [31, 32].

2.2 Graphene Preparations

Typically, there are two types of technology for graphene synthesis namely top-down and bottom-up methods. The first technology is called top-down because it involves obtaining single layer graphene sheets by breaking apart stacked graphene layers (i.e. graphite). The 'scotch tape' approach that Geim and Novoselov used to achieve their early graphene samples belongs to this technology [1]. As we know, graphite consists of staked graphene layers, hence, the peeling of graphene only requires to overcome the weak van der Waals forces between graphene layers [33]. That means preventing possible damage and re-agglomeration of the exfoliated sheets are the main challenges for this approach. Artificial graphite produced under high temperature [34] is not suitable for graphene exfoliation due to the poor graphitisation and non-uniform morphologies. Hence, several bottom-up methods have been developed to achieve graphene samples from other carbon sources. Unlike the top-down approach, bottom-up methods utilise carbon atoms to build the graphene sheet. The carbon atoms can be provided by various sources such as CH_4, C_2H_2 and C_2H_4. To achieve high levels of graphitisation, in the bottom-up approach, high temperature is usually preferred which guarantees the sample quality. The graphene synthesised with bottom-up method usually contains more defects than that achieved with top-down methods. However, relatively large-area graphene

sheets can be grown with the bottom-up method when proper substrate materials such as copper are used.

2.2.1 Top-down Methods

Top-down methods include mechanical exfoliation, graphite intercalation, nanotube slicing, pyrolysis method, etc. In this section, the most commonly used top-down methods are introduced and a discussion of their advantages and drawbacks is also presented.

2.2.1.1 Mechanical Exfoliation

Mechanical exfoliation might be the most well-known top-down method for graphene synthesis. It was first used by the Nobel Prize winners Geim and Novoselov to achieve single layer graphene [1]. The graphene films can be peeled from graphite using the so called 'scotch tape' method. Acetone is used to dissolve the tape with exfoliated graphene flakes. Then, the single and multilayer graphene is transferred to the substrate such as silicon for further study. As shown in Fig. 2.5, the monolayer graphene can be found under optical microscope among graphite flakes. So far, mechanical exfoliation remains the technology for high quality graphene synthesis. It is able to provide graphene sheets with size up to 100 μm [35], which is large enough for most of experimental studies and proof-of-concept devices. In fact, mechanical exfoliation has also been widely used in the synthesis of other 2D materials such as boron nitride and MoS_2 [36].

Jayasena et al. has improved the mechanical exfoliation by using ultrasonic-oscillations aided diamond wedge to scratch off the graphene [38]. This approach provides graphene layers with consistent properties through accurate control over the oscillations frequency and contact pressure. In terms of sample size, this technology does not seem to provide larger size than the manually exfoliated graphene. In another approach, the graphite is placed into stabilizing liquids such as sodium cholate and sheared at a rate of $> 10^4\,\mathrm{s}^{-1}$ [36]. Compared with Jayasena's method, this approach provides similar
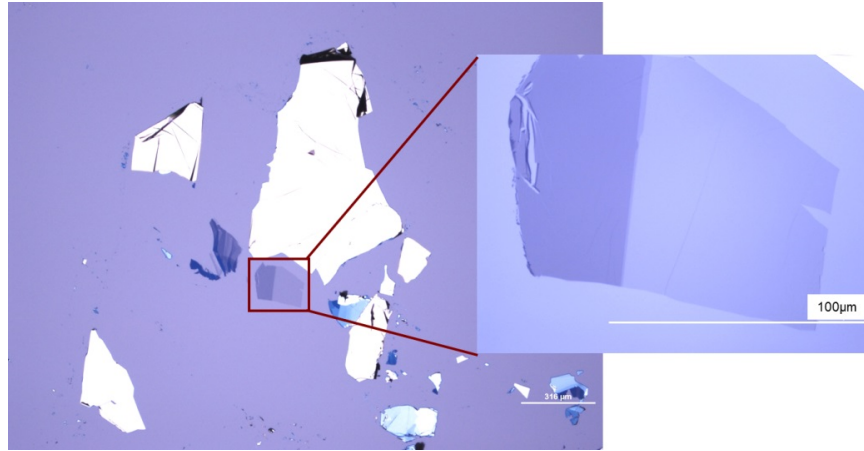
Figure 2.5: Exfoliated graphene layers under optical microscope with single layer region enlarged [37].

graphene quality and consumes less energy. The liquid used in this approach can also prevent graphene from oxidization.

2.2.1.2 Graphite Oxide Reduction

A lot of attention has been paid on the synthesis of graphene from graphite oxide (GO) [39–41]. This is because GO is easier to be exfoliated through sonication in water than graphite [42]. However, the exfoliated material is not graphene as it has been oxidised. Therefore, thermal or chemical treatment has to be implemented to reduce the oxide [43]. However, the resulting material after oxide reduction is generally named 'reduced graphene oxide' (rGO) rather than graphene due to the incomplete oxide reduction, resulting in different properties between rGO and graphene. It is also worth noting that the properties of rGO are different from graphene even for a complete oxide reduction due to the high level of defects induced during the synthesis of graphite oxide [33].

2.2.1.3 Other Top-down Methods

Besides the top-down methods introduced above, graphene can also be achieved from graphite intercalation [44–47]. The graphite intercalation compound (GIC) is produced

by inserting chemical species to the graphite interlayer, which increases their layer-to-layer distance and can potentially change the property of resulting material. It has been reported in [48] that alkali metal GICs could exfoliate spontaneously in N-methylpyrrolidone (NMP). Sonication can also be applied to assist and speed up the exfoliation. Other top-down approaches that have been reported are electrochemical exfoliation [49] and carbon nanotube unzipping [50, 51], etc. As they are not generally used in the synthesis of graphene transistors, they are not included in the discussion of this thesis.

2.2.2 Bottom-up Methods

The most popular bottom-up approaches for graphene synthesis are epitaxial growth and CVD. Other approaches such as the dry ice method [52] are not discussed in this thesis.

2.2.2.1 Epitaxial Growth on SiC

Epitaxial growth of graphene on SiC is one of the methods that can provide good graphene quality but with high cost as well. Graphene is grown epitaxially on the surface of SiC substrate in ultra-high vacuum (UHV). At a temperature of 1100 °C, silicon atoms on SiC sublimate and leave only carbon atom on the surface (graphitisation) [53], as shown in Fig. 2.6. This process can be slowed down with the presence of argon atmospheres [54–56] or small quantities of disilane [57], which allows higher temperatures to be used to improve the graphene quality. The most frequently used SiC substrate for graphene synthesis are 4H-SiC and 6H-SiC, which have hexagonal phase similar to the structure of graphene [58–61]. Due to the high cost of 4H-SiC and 6HSiC, cubic phase SiC has also been used for epitaxial graphene growth [62–64]. For electronic devices or circuits, SiC is a good insulting substrate that can be directly used after graphene synthesis. Therefore, the transfer step required in device fabrication with other synthesis methods is not needed. Due to the high temperature used to achieve
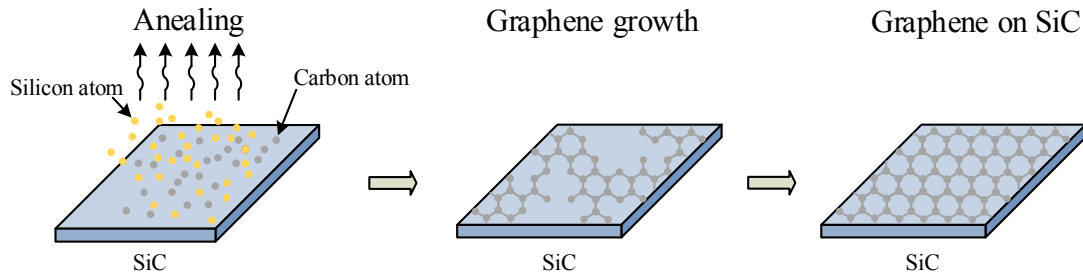
Figure 2.6: Epitaxial growth of graphene on SiC.

high quality graphene, a thin nickel layer has been implemented on the SiC surface to reduce the required temperature to 700∼800 °C [65]. In this case, graphene grows on the nickel surface rather than the SiC substrate, which generates additional cost of nickel and requires an extra transfer step from nickel surface to the insulating substrates for electronic applications.

The size of graphene grown with this approach depends on that of SiC wafer. The thickness and electronic properties of graphene also depend on the surface properties of SiC [66]. The weak anti-localization has been observed in epitaxially grown graphene in [67]. The mobility of graphene obtained with this approach is higher than CVD but lower than the exfoliated graphene [68].

2.2.2.2 Chemical Vapour Deposition

Due to the high cost and low yield of exfoliated and epitaxial grown graphene, CVD has been applied to synthesis mono- and multilayer graphene. CVD has been widely used in the semiconductor industry for the deposition of thin films like polycrystalline silicon [69, 70] and silicon dioxide [71, 72]. It has also been used to synthesis nano materials such as carbon nanotubes [73] and ZnO nanowires [74]. The idea of synthesis graphene using CVD methods can be tracked back to the 1970s. Graphene was grown on the surface of crystalline nickel and characterised directly on the substrate without transfer [75, 76]. Thus, extraordinary electronic properties of graphene such as ultrahigh carrier mobility were not observed. In 2009, Reina et al. successfully transferred large-

scale CVD graphene from a polycrystalline nickel covered substrate to silicon dioxide substrate [77]. A similar work was also reported by Kim et al. [78] in the same year, bringing an upsurge of interest in CVD graphene synthesis.

There are three main aspects in CVD graphene growth, namely carbon source, substrate and growth conditions (e.g. pressure, temperature). The most commonly used carbon sources are straight-chain alkanes such as methane (CH_4), ethylene (C_2H_4) and acetylene (C_2H_2). The growth temperature is mainly determined by the decomposition rate of the carbon source. Reduced gas (H_2) and noble gas (Ar, He) or the mixing of them are often used during the CVD process. So far, graphene has been reported to grow on various metallic substrates like nickel [77, 78], copper [79, 80] and ruthenium [81, 82], as shown in Fig. 2.7. Poly(methyl methacrylate) (PMMA) is the most frequently used material to transfer CVD grown graphene to arbitrary substrate. As shown in Fig. 2.7, after graphene deposition the PMMA is spin-coated on the graphene/metal substrate. Then the copper is etched away, forming the graphene/PMMA film to be coated onto the desired substrate. At the end, the PMMA is also washed away by acetone, leaving only graphene on the top of the substrate.

According to the mechanism during the composition of graphene, the CVD methods can be split into two types namely surface-catalysed and segregation. In the former case the carbon source decomposes and releases carbon atoms that deposit on the metal (e.g. Cu) surface and form self-limiting mono-layer graphene islands. These graphene islands not only prevent the formation of multilayer graphene but also gradually grow larger and connect with each other to form large scale graphene. Due to the different lattice orientation in the graphene islands, defects are formed at the boundaries when the islands connect to each other, resulting in polycrystalline graphene [83].

Compared with the surface-catalysed approach, the segregation method has its advantage in producing crystalline graphene. In 2009, crystalline graphene with millimetre scale was successfully synthesised on crystalline ruthenium substrate under UHV and 1000 °C [84]. In this mechanism, carbon atoms dissolve into the substrate under high
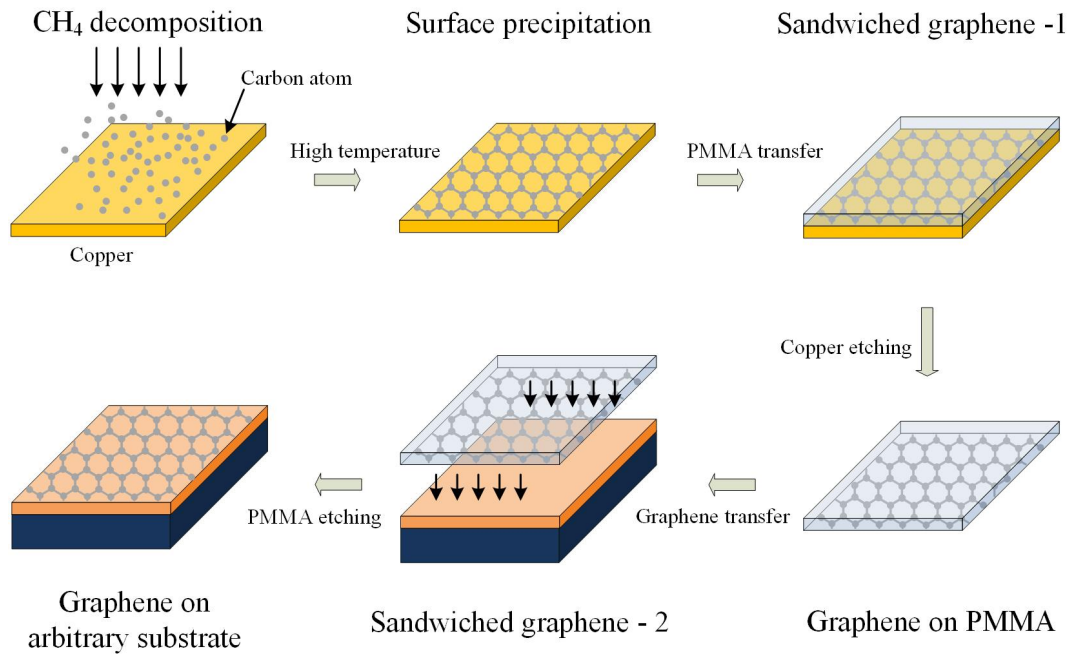
Figure 2.7: CVD growth of graphene and transferring onto arbitrary substrate.

temperature and diffuse to the metal surface to form graphene during the cooling process. The number of graphene layers heavily depends on the cooling rate and the size of crystalline graphene achieved is smaller than surface-catalysed polycrystalline graphene. In addition, the strong interaction between graphene and ruthenium limits the transfer of graphene to other substrates. Moreover, the high cost of crystalline ruthenium substrate is not financially viable for mass production either.

2.3   Graphene Transistors

In 1947, the first transistor based on crystal germanium (Ge) was expermentally demonstrated at Bell Labs by John Bardeen and Walter Brattain. Today, the invention of transistor is considered as the one of the most important events in the last century and has also been named as an IEEE milestone in 2009 [85]. Transistor is an active component that plays the key role in almost all electronic devices. Its ability of mass production enables the wide implementation of transistor-based electronics today. While

there is still billions of demand for discrete transistors every year, most of the transistors are produced in integrated circuits with nanoscale dimensions now. They work together with other components such as diodes and capacitors to achieve the designed function. Although the research and development of integrated circuits are costly, the averaged cost of each chip out of the millions of mass-produced chips can be extremely low. The number of transistors in today's advanced microprocessor can reach a few billion [86]. According to Moore's law, this number should be doubled every two years, which unfortunately is not true now as the size scaling of Si MOSFET has slowed down according to the annual report of Intel in 2015 [87]. The fact that Moore's law is dying in the next decade and the limit of silicon technology introduce a strong demand for the development of next generation high speed transistors. Before the discovery of graphene, the carbon nanotube, sometimes also considered as the rolled form of graphene, has been proposed as the potential material to develop nanoscale transistors beyond silicon [88]. However, the high production cost and lack of technology for mass production have limited their applications in semiconductor industry. With nominal carrier mobility of 10,000~15,000 cm^2/Vs [1] measured in few-layer exfoliated graphene on SiO$_2$ substrate at room temperature, graphene is considered as one of the most promising channel material for fast transistors since its discovery. In fact, the measured record room-temperature mobility exceeding 100,000 cm^2/Vs has been reported in h-BN encapsulated graphene at a carrier density of 10^{11} cm^{-2} [18], far beyond that of any known semiconducting materials.

Since the first top-gated GFET reported in 2007 [89], thousands of graphene transistors have been fabricated and measured. Conventional GFET utilizing relatively large-area graphene as well as FETs with GNR and bilayer graphene has been proposed. The tunable bandgap in GNR and bilayer graphene FETs enables the possibility for digital applications. Besides these lateral structures, the graphene-based vertical transistor configurations have also been proposed. Vertical tunnelling mechanisms are implemented in these devices, drastically improving their switching performance. In this section, the graphene transistor classification shown in Fig. 2.8 will be reviewed. In order to
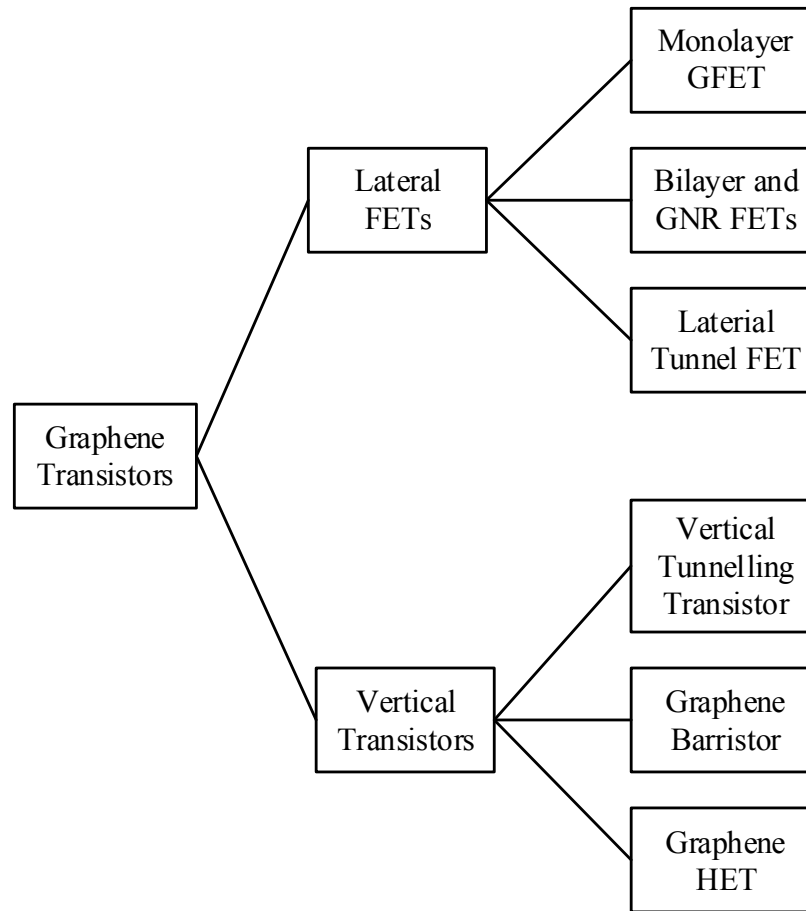
Figure 2.8: Classification schemes for graphene transistors.

make a fair comparison between graphene-based and other transistors, it is necessary to introduce some important transistor figures of merit (FoMs) before the review.

2.3.1   Transistor Figures of Merit

As we know, there are two basic functions for transistor namely switching and amplifying. In the former case, transistor is used as a current switch that controls the current flow through the gate (or base) bias. Take FET for example, in logic circuits FETs act as electronic switches switching between on and off states to realize the logic functions. When a FET is off, no current can flow through the channel and the energy consumption is negligible. When a FET is on, it allows large current to flow through the channel

and the transistor works as a variable resistor in its triode (linear) region. Thus, the important figures to judge the switching behaviour are the off-state current and on-off current ratio. Apparently the smaller the off-state current is, the less static power the FET consumes. Low static power dissipation is extremely important not only for portable devices which suffer from the short battery life, but also for the non-portable systems to reduce self-heating and save energy. Besides, the on-off ratio is also an important figure that determines whether the FET can be used for logic circuits. Modern digital circuit usually requires a minimum on-off current ratio of 1,000~10,000 [90].

Low off-state current and high on-off current ratio are basic requirements for an electronic switch. In computer processors, the switching speed of FETs is an important factor. Higher switching speed means low logic delay which allows the use of higher clock frequency to improve the processor speed. Faster response to the gate bias variations can be achieved by scaling the gate length or using channel material with high carrier mobility. As the scaling of Si MOSFET has slowed down due to the appearing of more significant short-channel effects such as threshold-voltage roll-off and drain-induced barrier lowering, current integrated circuits are approaching very closely to the limit of silicon technology. The scale length (λ) is often used to evaluate the gate scalability of a FET. It is originated from the silicon technology but has been used for graphene transistors as well [91, 92]. Scale length reflects the ability of a FET to fight against the short-channel effects.

Subthreshold swing S describes the relation between drain current and gate bias. It is defined as the gate-to-source voltage needed to vary the drain current by a factor of 10 in the subthreshold region of a FET (e.g. $V_{gs} < V_{to}$ for n-type FET, where V_{to} is the threshold voltage). The unit of S is mV/dec. Obviously, in practice a small S is desired and the maximum acceptable value is 60 mV/dec for Si MOSFETs, beyond which a large supply voltage is needed that increases the power dissipation [93].

In analog/RF circuits, the amplifying property of transistors is used. There are three basic types of amplifier namely common-source (CS), common-drain (CD) and common-

gate (CG) for FETs, corresponding to common-emitter (CE), common-collector (CC) and common-base (CB) for BJTs. In the linear region of a CG amplifier, when a small RF signal is applied to the gate, the quantity of channel carriers changes and so does the channel current. As a result, an amplified RF signal with identical frequency but higher amplitude appears at the drain. Typically, transistors in amplifiers are biased at active region and the DC operating point is usually chosen in the middle of the load line. During the amplifying procedure, there is no need to switch the transistor off. Therefore, for analog/RF circuit the designer are only concerned about the amplifying behaviour rather than the switching performance.

To describe the characteristics of a transistor for amplifying, parameters including intrinsic voltage gain (G_{int}), current gain (h_{21}) and unilateral power gain (U) should be introduced. As shown in Fig. 2.9, the simplified small-signal model of a FET is presented. g_m is the transconductance and g_{ds} is the drain conductance. C_{gs} and C_{gd} are the gate-source and gate-drain capacitances. R_s, R_d and R_g are the source, drain and gate resistances respectively. R_i is the gate-charging resistance induced by the gate dielectric. G_{int} is defined as the ratio g_m/g_{ds}. It is the maximum voltage gain that can be achieved with the transistor and is independent of the frequency of operation. h_{21} and U take into consider the frequency response and decrease monotonically against frequency at a slop of -20 dB/dec. The frequency when current gain equals to 1 is called cutoff frequency (f_T) and the frequency when unilateral power gain reaches 1 is named maximum frequency of oscillation (f_{max}). In applications such as power amplifiers, f_{max} is more important than f_T as above this frequency the transistor does not provide power gain. The expressions of f_T can be derived from the small signal model as [90]:

$$f_T = \frac{g_m}{2\pi \left((C_{gs} + C_{gd}) \left[1 + g_{ds} \left(R_s + R_d \right) \right] + C_{gd} g_m \left(R_s + R_d \right) \right)}, \tag{2.2}$$

Apparently, higher f_T can be achieved by minimizing the capacitances (C_{gs} and C_{gd}) and resistances (R_s, R_d and g_{ds}) and maximizing g_m. The expression of g_m in saturation region of MOSFETs (i.e. $I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$) can be approximately written as

Intrinsic FET
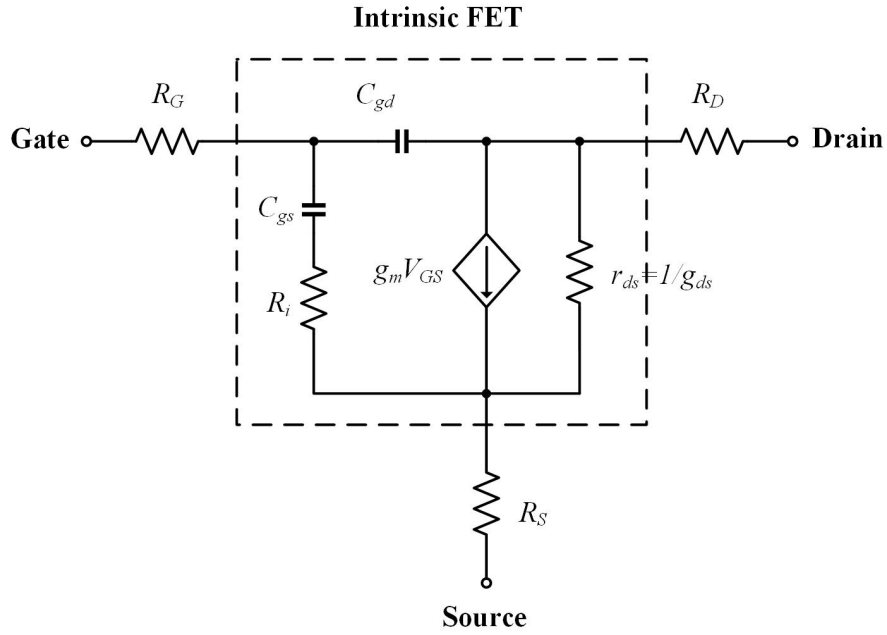
Figure 2.9: Typical small signal model of a FET.

[94]

$$g_m = \frac{dI_D}{dV_{gs}}\bigg|_{V_{ds}=\text{cnst}} = \mu C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right) \tag{2.3}$$

where W is the channel width, μ is the carrier mobility and C_{ox} is the gate oxide capacitance density and V_t is the threshold voltage. Obviously, higher carrier mobility gives higher g_m, hence, higher f_T. In term of f_{max}, the expression has been derived as [95]

$$f_{max} = \frac{f_T}{2\sqrt{\left(R_g + R_i + R_s\right)g_{ds} + 2\pi f_T C_{gd}R_g}}, \tag{2.4}$$

Apparently, improving f_{max} also requires to reduce the resistances and gate capacitance. It is worth mentioning that both f_T and f_{max} are sensitive to the bias condition therefore it is also important to bias the transistor at the optimum operating point. It is also noted that in Eq. (2.2) and (2.4), the external parasitics that heavily depends on the fabrication process are included. To make a fair comparison by excluding the effects of external parasitics, the intrinsic cutoff frequency f_{T-int} and maximum frequency of

oscillation $f_{max-int}$ are also proposed [93]

$$f_{T-int} = \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)},$$ (2.5)

$$f_{max-int} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds} R_i}}.$$ (2.6)

In practice, f_{T-int} and $f_{max-int}$ can be de-embedded from the measurements.

According to Eq. (2.5) and (2.6), f_{T-int} and $f_{max-int}$ can be improved by channel length scaling (i.e. reducing C_{gs} and C_{gd}) and utilising channel material with high carrier mobility (i.e. increasing g_m). To match the electrostatic requirements of short-channel FETs, thin gate dielectric and atomic thin-channel material are desirable [91]. As an atomic thick material with measured room-temperature carrier mobility exceeding 100,000 cm^2/Vs on h-BN [18], graphene is definitely a promising candidate for short-channel high speed FETs. Compared with the carrier mobilities of few hundred cm^2/Vs in Si MOSFETs, $\sim$6000 cm^2/Vs in GaAs pseudomorphic high-electron-mobility transistors (pHEMTs) [96] and exceeding 10,000 cm^2/Vs for InP high-electron-mobility transistors (HEMTs) [97] and GaAs metamorphic high-electron-mobility transistors (mHEMTs) [98] [90], this ultrahigh mobility of graphene is better by at least a factor of 10.

As we know, graphene is a gapless material whose conduction and valence bands form conical energy spectrum at the K points of the Brillouin zone. When the Fermi level is shifted to the upper half of the Dirac cone by external electric field (or chemical doping), the electrons become the major carriers in graphene and conduct current under proper bias voltage. On the other hand, if the direction of external electric field is reversed, the Fermi level is shifted to lower half of the Dirac cone and the major carriers become holes. At the Dirac point, there are still free electron-hole pairs stops the graphene FET from switching off. The fact that graphene allows both electrons and holes as the major carriers lead to the so-called ambipolar conduction property of GFET. The high carrier sheet density of graphene in excess of 10^{12} cm^{-2} is able to provide enough carriers for

appropriate current conduction, resulting in potentially high g_m for f_{T-int} and $f_{max-int}$ improvement.

2.3.2 Monolayer Graphene Field-Effect Transistor

In this section, the conventional GFET consists of large-area monolayer graphene is discussed. As there are also GNR and bilayer graphene FETs, the GFET in the rest of this thesis means conventional GFET unless otherwise stated. The electric field effect in graphene has been reported with its discovery in 2004 [1]. Novoselov and Geim demonstrated the first back-gated graphene device on 300-nm SiO_2-coated silicon substrate. As a proof-of-concept device, this FET configuration suffers from the large parasitic capacitances induced by the back-gate structure, which also limits the integration of GFET with other components. In 2007, the top-gate GFET were reported by [89] as a significant step towards mass production. Thanks to the CMOS-compatible top-down process flow used, the research in graphene transistor has been developed rapidly in the past decade. Dual-gate GFET configuration, as shown in Fig. 2.10(a) and (b), have also been reported later [99–101], enabling investigation for the access resistance caused by the area of graphene that are not covered by the top gate. As these graphene areas are exposed in the air, their resistances cannot be effectively modulated in a top-gate device. High access resistance can significantly degrade the performance of top-gate devices. It has been reported in [101] that large access resistance reduces the intrinsic cutoff frequency of GFETs.

So far, GFETs with exfoliated [1, 99–102] as well as CVD [103, 104] and epitaxially grown graphene [105–107] have been investigated. The top-gate material varies from SiO_2 [89] to emerging high-k dielectrics such as Al_2O_3 [99–101] and HfO_2 [102, 107]. Due to the gapless bandstructure of graphene, these devices exhibit poor on-off ratio that do not satisfy the requirement of digital circuits. Meanwhile, the carrier mobility of graphene in these transistors is also degraded by the substrate and top-gate dielectric (1000~8000 cm^2/Vs). As shown in Eq. (2.3) and (2.5), g_m and f_{T-int} are positively proportional
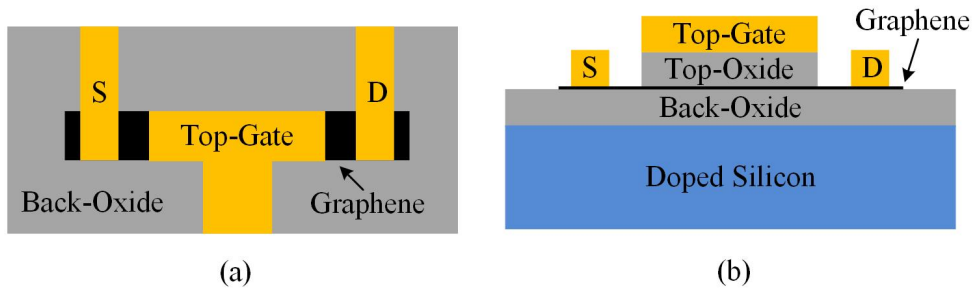
Figure 2.10: Conventional GFET schematic (a) top view (b) cross-sectional view.

to the carrier mobility. Consequently, higher f_{T-int} can also be achieved by scaling the channel length. Therefore, in order to achieve high f_{T-int} out of GFET, it is important to retain the high carrier mobility of graphene and reduce the channel length. Following this guidance, in 2008 the first gigahertz GFET with an intrinsic cutoff frequency of 14.7 GHz was presented [108], which has a channel length of 500 nm. Later in 2009 the GFET demonstrating f_{T-int} of 50 GHz was achieved by scaling the gate length to 350 nm [109]. A 240-nm-long GFET exhibiting 100-GHz f_{T-int} was reported in 2010 [110] and in the same year 300-GHz f_{T-int} was measured with a 144-nm gate GFET [111]. As the mobility of graphene is significantly degraded by the defects introduced during the top gate deposition, this 300-GHz GFET utilises peeled graphene and a self-aligned nanowire gate, as shown in Fig. 2.11 to prevent the possible damage and retain the high carrier mobility of graphene. Compared with the work of [112] utilizing a gate length as short as 40 nm to achieve 350-GHz f_{T-int}, this self-aligned nanowire gate greatly improves f_{T-int} without further scaling the gate length. In 2012, a GFET with mechanically exfoliated graphene and 67-nm self-aligned nanowire gate was reported, demonstrating the state-of-the-art f_{T-int} of 427 GHz [113]. Hence, the f_{T-int} of GFET is competitive with the best InP HEMTs and GaAs mHEMTs at comparable channel lengths [93]. With carrier mobility in excess of 100,000 cm^2/Vs, the h-BN encapsulated graphene can potentially improve the f_{T-int} of GFET to THz region.

Generally, the $f_{max-int}$ of a FET is close to (e.g. Si MOSFETs) or higher than (e.g. InP HEMTs, GaAs mHEMTs and GaAs pHEMTs) f_{T-int}. Although conventional
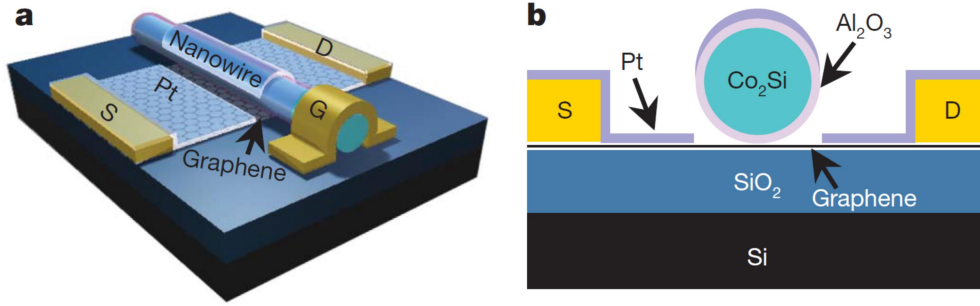
Figure 2.11: GFET with self-aligned nanowire gate (a) three-dimensional view (b) cross-sectional view [111].

GFETs have demonstrated measured f_{T-int} exceeding 400 GHz, their intrinsic maximum frequency of oscillation $f_{max-int}$ is significantly smaller due to the lack of drain current saturation, as shown in Fig. 2.12. The typical $f_{max-int}$ of GFETs reported are 30~200 GHz [112, 114–119], drastically lower than the 1.2 THz reported for the 35-nm-long InP HEMTs [120]. From the expression in Eq. (2.4), f_{max} can be increased by minimizing resistances R_g R_i and R_s. The gate resistance R_g is actually the main reason for high f_T and low f_{max} in Si MOSFET before year 2000 [121]. However, from Eq. (2.6) it can be seen that $f_{max-int}$ is free from R_g but inversely proportional to the square root of drain conductance

$$g_{ds} = \frac{1}{r_{ds}} = \frac{\partial I_{ds}}{\partial V_{ds}}\bigg|_{V_{gs}=\text{const}} \tag{2.7}$$

where r_{ds} is the output resistance. In order to achieve high $f_{max-int}$, g_{ds} has to be reduced which requires saturation current. As as f_T and f_{T-int} are independent of g_{ds}, the poor saturation current does not affect the cutoff frequency of GFET.

Since GFET has demonstrated comparable cutoff frequency to the best III-V HEMTs at similar channel length, a great deal of efforts have been paid on improving their saturation current for high frequency applications. In 2008, GFETs with saturation behaviour were experimentally demonstrated by Meric et al. [122]. Their model reveals that the mechanism of drain current saturation in GFET is different from that of Si MOSFETs or III-V HEMTs [122]. Theoretical study presented by Han et al. suggests the utilization of thin gate dielectric to improve the saturation behaviour of GFET
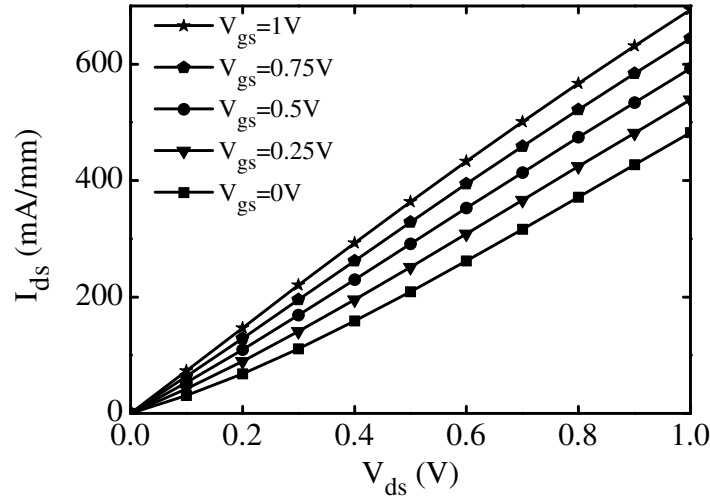
Figure 2.12: Typical output characteristics of a GFET.

[123]. They attribute this improved drain current saturation to the better electrostatic gate control over channel charge density when a thin gate dielectric is implemented. Later in 2012, it was reported by Wu et al. that GFETs can also demonstrate negative differential resistance (NDR) under certain biasing condition [124]. They explained this unique behaviour of GFET with the qualitative channel charge distribution shown in Fig. 2.13. Assume the graphene is undoped and $V_{gs} > 0$, when $V_{ds} = 0$ the channel would be purely n-type, as shown in Fig. 2.13(a). If a positive voltage is applied to the drain ($0 < V_{ds} < V_{gs}$), the charge density on the drain end decreases. As V_{ds} is increased to the condition $V_{ds} = V_{gs}$, the channel would be virtually pinch-off (as the GFET cannot be completely switched off) at the drain edge, as shown in Fig. 2.13(b). Apparently, the overall channel resistance in 2.13(b) is higher because of the reduced charge density at the drain end. The maximum channel resistance is achieved when the pinch-off point is moved to the middle of the channel, as shown in Fig. 2.13(c), where, instead of unipolar electron channel, right half of the channel is dominated by holes. This increase in the overall channel resistance can potentially cause NDR behaviour. Following this work, Sharma et al. quantitatively revealed the mechanism behind the saturation current and NDR behaviour of GFET with their drift-diffusion model in 2015 [125]. It is also noted that the NDR phenomenon favours a thinner equivalent oxide
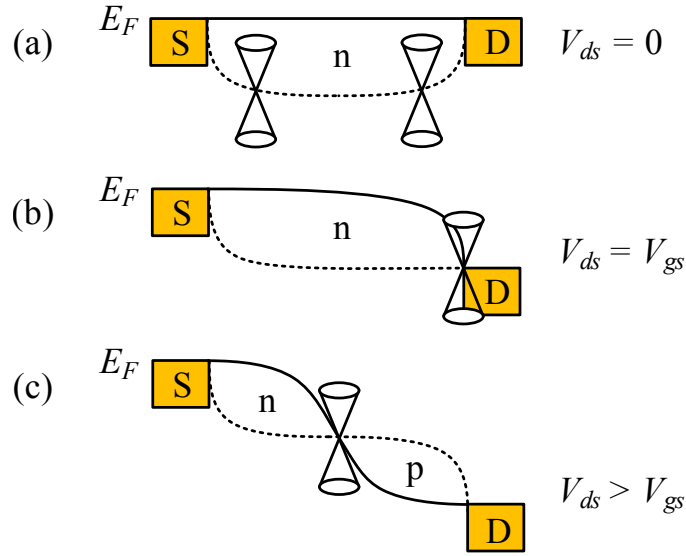
Figure 2.13: Qualitative charge distribution in the graphene channel for constant gate-to-source voltage and (a) $V_{ds} = 0$ (b) $V_{ds} = V_{gs}$ (c) $V_{ds} > V_{gs}$. The Dirac cone represents the charge neutrality point.

thickness due to the larger drop rate of average channel charge density in these devices [125]. Meanwhile, the drain current saturation and NDR behaviour are general features of GFETs that are not limited by the synthesis method of graphene or type of gate dielectric materials used. In addition, the effect of drain source series resistances is also conducted in Sharma's work. It is observed that R_s and R_d can significantly degrade the saturation and NDR behaviour of GFET. Their experimental results show that a GFET, with NDR phenomenon fully shadowed by the large series resistances, exhibits restored NDR behaviour when a back gate was employed to reduce R_s and R_d. In practice, R_s and R_d can also be decreased by reducing the contact resistance between graphene and the metallic electrodes. The contact resistances in many reported graphene devices (400~1000 $\Omega/\mu m$) are usually ten times that of the silicon or III-V transistors [126]. It has been experimentally demonstrated that resistance as low as 69 $\Omega/\mu m$ can be achieved for Pd/graphene contact [127], representing the state-of-the-art contact resistance between graphene and metal electrodes.

2.3.3 Bilayer and GNR FET

In order to improve the on-off current ratio of GFET, it is necessary to open a bandgap in graphene. Quantum mechanical calculations have predicted the opening of a field-induced bandgap in Bernal-stacked large-area bilayer graphene [128, 129]. The electric field is applied perpendicularly to the bilayer graphene sheet through the top and back gates, resulting in different excess charge density on each layers and breaking the symmetry of charge density between two graphene layers. This asymmetric charge density introduces Coulomb interaction between the graphene layers, resulting in the opening of a bandgap between the conduction and valence bands. Theoretical calculations have predicted a bandgap as high as 300 meV under the electric field of a few V/nm [128–130]. The actual measured bandgaps in bilayer graphene are only up to 130 meV [131, 132]. As these bandgaps are much smaller than the desired 360-500 meV for logic circuits, the maximum measured on-off ratio of these bilayer graphene FETs is limited to approximately 100 [90, 133, 134]. On the other hand, it is reported in [135] that bilayer graphene FETs exhibit better drain current saturation compared with the conventional GFETs due to the existence of a bandgap. Their bilayer graphene FETs demonstrate an intrinsic voltage gain of 35, higher than that of their conventional GFET by a factor of 6. However, the large parasitic capacitances induced by the back gate can potentially degrade the performance of bilayer graphene FETs at high frequencies.

An alternative approach to open a bandgap in graphene is to reduce its width to nanometer scale. As depicted in section 2.2.1, there are zigzag and armchair GNRs depends on the shape of their edge. Zigzag GNRs are always semimetal with zero bandgap like large-area graphene but armchair GNRs show width dependent bandgap that is promising for semiconductor applications. While Yang et al. [136] attribute this sizeable bandgap to the lateral confinement induced by the armchair edges, Sols [137] and Han [138] suggest that other effects such as Coulomb blockade are also important in the generation of a bandgap. It has been predicted with first-principle calculations in [136] that the gap size is inversely proportional to the width of GNR and by reducing the width

below 2 nm a bandgap up to 1 eV can be achieved. Due to this large bandgap, the on-off ratio of GNR FETs can potentially match the requirement of digital applications. In 2008, Li et al. reported their back-gated p-type GNR FETs with sub-10 nm width [139]. Measured bandgap up to 400 meV and on-off ratio up to 10^7 have been demonstrated regardless of the GNR edge roughness, which was thought can degrade the on-off ratio by increasing the off-current and lowering the on-current [140, 141]. However, the large subthreshold swing caused by the thick back-gate dielectric has to be reduced for practical applications. Meanwhile, complementary logic circuits also requires the n-type GNR FETs with excellent switching behaviour and acceptable subthreshold swing, which has not been demonstrated yet. Moreover, the fabrication of well-defined GNRs is not easy for today's technology and the variations in graphene quality can also limit the mass production of GNR FETs.

Except these conventional bilayer graphene and GNR FETs, another type of lateral transistor that can provide large on-off ratio for digital circuit applications is the lateral graphene tunnel FET. It is noted that all the graphene FETs introduced so far are based on the gate tuning of channel carrier density. The switching of tunnel FET, on the other hand, is realised by employing gate control over the band-to-band tunnelling of carriers from source to drain. In fact, there are also other tunnel FETs utilizing non-graphene channel materials [142]. As the channel material with a reasonable bandgap is needed, tunnel FETs utilizing both GNR and bilayer graphene have been explored with quantum mechanical simulations [143–145]. On-off ratio up to 10^4 has been predicted with these theoretical calculations and the subthreshold swing as small as 20 mV/dec is predicted, much smaller than the 60 mV/dec limit of Si MOSFETs. In addition, the tunnel FETs also exhibit a low off-current that can help to reduce the static power dissipation [145]. Moreover, it is noted that bilayer graphene, although with a smaller bandgap, seems to be a better option for tunnel FETs due to the immature fabrication process of GNRs. Thanks to the low substhreshold swing, high on-off ratio can be possibly achieved with reasonable gate voltage regardless of the small bandgap in bilayer graphene.

While a bandgap is open in bilayer graphene and GNRs, unfortunately, it has been observed that the carrier mobility decreases dramatically as a side effect. In other words, the bandgap is achieved at the cost of lower carrier mobility. In [93], it has been summerised that the carrier mobility is roughly inversely proportional to the width of the bandgap. This relation applies not only to bilayer graphene and GNRs but also to Si, CNT and III-V devices. Thus, in order to achieve a on-off ratio of $10^4 \sim 10^7$, the GNR width has to be smaller than 10 nm, which unfortunately degrades the carrier mobility to less than 1000 cm^2/Vs [93, 139].

2.3.4 Vertical Graphene Transistors

As depicted in Fig. 2.8, graphene transistors can be divided into lateral and vertical devices depending on the geometry. The graphene FETs discussed in the previous sections are all lateral devices, in which the current flows along the graphene sheet. The vertical graphene transistors, on the other hand, are based on tunnelling mechanism similar to that of the lateral tunnel FETs. In these devices, barriers are vertically sandwiched between the electrodes and the current flows perpendicularly to the graphene sheet. According to the type of barriers and device structure, several concepts have been developed for vertical graphene transistors theoretically or experimentally.

In early 2012, the first experimental work of vertical graphene transistor based on quantum tunnelling mechanism was demonstrated [146]. As shown in Fig. 2.14, this transistor utilizes the heterostructure of graphene and another 2D material h-BN, with graphene encapsulated between the h-BN layers to retain its extraordinary electronic properties. The electrodes are semimetal graphene and h-BN acts as the insulating barrier allowing carriers to transport through with a probability determined by the bias voltage V_b between the graphene electrodes. The back-gate voltage V_g, on the other hand, tunes the density of states (DoS) in graphene. As the DoS determines the available number of states that can be occupied for each energy level, tuning the DoS would result in efficient modulation of the current flowing between the graphene electrodes. The
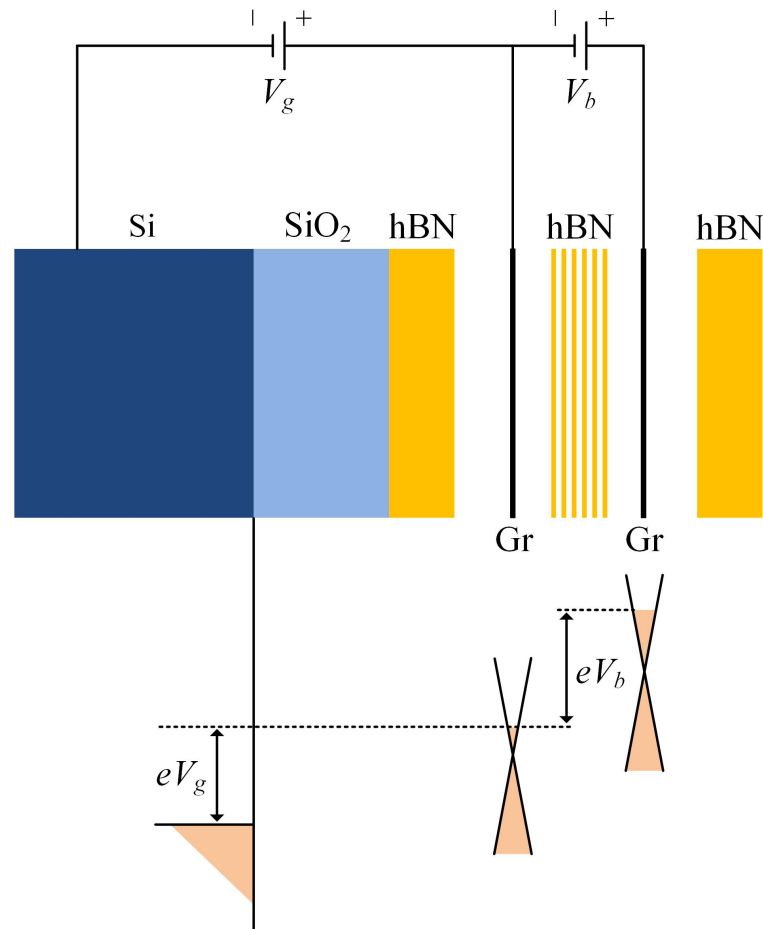
Figure 2.14: Graphene field-effect tunnelling transistor and the corresponding band structure.

maximum measured on-off ratio of the vertical graphene-h-BN tunnelling transistors are about 50. To improve the on-off ratio, the insulating h-BN with a bandgap of 5.2 eV is replaced with the semiconducting MoS_2, whose bandgap varies from 1.95 to 1.2 eV when the thickness is reduced from bulk to monolayer. As the tuning range of Fermi energy E_F in graphene is close to the bandgap of MoS_2, more effective barrier height modulation was achieved compared with the graphene-h-BN counterpart. On-off ratio of the graphene-MoS_2 tunnelling transistor as high as 10^4 has been measured. The next year, the vertical graphene transistors with WS_2 barrier were reported as well, demonstrating a on-off ratio up to 10^6 [147]. In addition, the negative differential conductance was also observed in devices with h-BN barrier at high V_b regime [148].

In middle 2012, Yang et al. proposed another type of vertical transistor called graphene barristor [149]. As shown in Fig. 2.15, it consists of a graphene source and silicon drain, with top gate synthesised on the top of the graphene/silicon contact area. The mechanism behind this barristor is the gate-induced modulation on the Schottky barrier formed between graphene and doped silicon due to their different work functions. As the work function of graphene can be tuned electrostatically by the top gate voltage, the height of the Schottky barrier is also modulated. Complementary logic switches can be achieved using p- and n-type silicon, corresponding to the p- and n-type barristor respectively. The authors demonstrated a maximum reverse-biased on-off ratio of 300 and a forward-biased on-off ratio up to 10^5 with their p-type barristors, exceeding the minimum requirement of digital circuits. The barristor exhibits small off-state current thanks to the high Schottky barrier achieved and the devices is also capable of carrying large current density. The complementary barristors-based inverter and half-adder were also demonstrated, regardless of the poor performance due to the non-optimized device dimension and fabrication process.

2.3.5 Hot-Electron Transistor

It is noted that the vertical graphene transistors introduced so far are aiming at high on-off ratio for logic applications. As their output characteristics do not exhibit saturation behaviour, these devices are not suitable for analogue/RF applications. It has been theoretically predicted in [150] that the hot-electron transistor (HET) with a graphene base can provide excellent DC and RF behaviours. The concept of HETs were developed back to the 1960s [151]. Similar to BJTs, HETs consist of three regions namely emitter, base and collector, separated by emitter-base insulator (EBI) and base-collector insulator (BCI) respectively. The hot electrons are injected from emitter to base across the EBI and are eventually collected at the collector across the BCI. The thick metallic base used in conventional HET introduces strong scattering to the carrier transport from emitter to collector and increases the base transition time, lowering the cutoff frequency
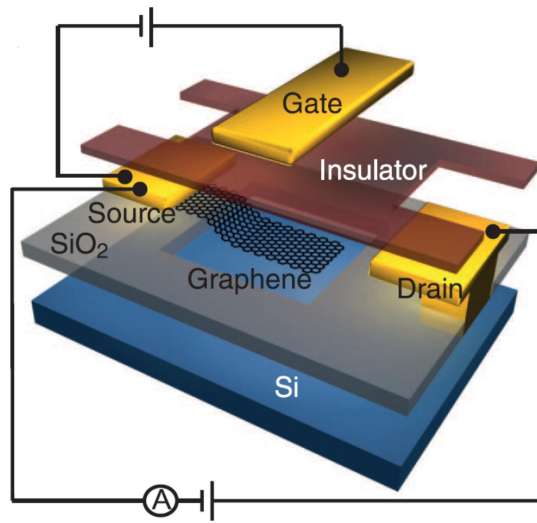
Figure 2.15: Schematic of graphene barristor [149].

of the conventional HET. Reducing the metallic base material can decrease the transition time but at the same time increase the base resistance. Therefore, although HETs are theoretically predicted to exhibit high cutoff frequency, the thick base material and non-ideal fabrication process limit their applications at high frequencies.

Due to the atomic thickness and excellent electrical conductivity, graphene is considered as an ideal base material for HETs. It does not affect the vertical transport of electrons and is able to provide low base resistance for high speed device. In early 2013, HETs with graphene base were fabricated and measured for the first time [152]. These HETs were synthesised with CMOS-compatible process utilizing nanometer thick SiO_2 as EBI material and Al_2O_3 as BCI material. While simulations predict good on-off ratio and saturated output current [150], the experimental results show a on-off ratio up to 10^4 without saturation behaviour. Meanwhile, most of the emitter current flows to the base rather than the collector, resulting in a low transfer ratio $\alpha = I_C/I_E$ of 6.5% only. The authors attribute the poor performance of their HETs to the non-optimized thickness and material selection of EBI and BCI. This was confirmed later by Zeng at al. [153] in the same year. Their measurement results show a maximum effective transfer ratio of $\alpha^* \approx 44\%$ as well as excellent saturation current. In addition, their devices

also demonstrate the state-of-the-art on-off ratio of 10^5 for graphene HETs. As none of these measured graphene HETs can demonstrate performance good enough for practical applications, the potential of graphene HETs remains to be explored.

2.4 Conclusion

In this chapter, the electronic, optical, mechanical and thermal properties of graphene have been briefly introduced. The approaches for graphene preparation including mechanical exfoliation, graphene oxide reduction, epitaxial growth on SiC and CVD are also depicted. Based on these knowledge, a review of graphene transistors are also conducted. The figures of merit of a FET as well as the concept of lateral and vertical grahene-based transistors are included. Besides the graphene transistors introduced in this chapter, there are also a few concepts for vertical graphene transistor that are theoretically studied only. For instance, Lecce et al. calculated the performance of an graphene-base heterojunction transistor utilizing the graphene/semiconductor Schottky barriers instead of EBI and BCI [154]. A high on-off ratio of 10^4 and current saturation behaviour have been predicted along with a high cutoff frequency exceeding 1 THz. As no experimental results are available at the moment, the potential of these concepts cannot be assessed and are not discussed in this thesis.

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Chapter 3

GFET Modelling

Modelling of graphene transistors is important for the exploration of device and circuit performance as it provides a time-efficient low-cost approach for materials and technology investigations. An accurate modelling approach can be greatly helpful to the selection of material and technology during the device design. With the size scaling of graphene devices, it is necessary to develop multiphysics and multiscale modelling approaches to achieve a tradeoff between accuracy and computing time. In this chapter, an overview of existing multiscale modelling approaches is presented, followed by the detailed derivation of a novel analytical GFET model for circuit analysis.

3.1   Multiscale Modelling of Graphene Transistors

The multiscale modelling approaches have been divided as *ab initio*, atomistic modelling, semiclassical device modelling and analytical modelling [1]. With the tradeoff between accuracy and computational cost in mind, these approaches utilise different methods to model the performance of graphene transistors. The main challenge of multiscale modelling is to accurately define the *ad hoc* level hierarchies and information exchange interfaces between the multiscale systems.

3.1.1 *Ab initio* **Modelling**

A model is from *Ab initio*, or first principles, if it originates from the established science without using assumptions like empirical parameters. *Ab initio* modelling is the most time consuming method among these approaches. It is based on the solving of wavefunction utilizing Hartree-Fock self-consistent field or mean-field approximation [2–4], from which the fundamental quantities of a material such as effective masses, energy gaps, metal work functions, electron affinities, and scattering rates can be extracted. As carbon atoms have relative simple chemical properties, larger systems can be simulated with the quantum chemistry tools such as VASP [5], ATK [6], QUANTUMESPRESSO [7], ONETEP [8], AB-INIT [9]. These *ab initio* simulators allow parallel computation in clusters with linear scaling, thus, can be used to simulate relatively large-scale devices.

Density functional theory (DFT) that computes one-body electron density instead of many-particle wave functions has been an effective first-principle approach for semiconductor device simulation [1]. One of the advantages of DFT is the good accuracy in predicting the DoS for transportation calculation. It also provides good accuracy in the calculation of thermodynamic properties of solids [10]. However, it fails in the estimation of chemical reactions barriers, the energies of charge transfer excitation and dissociating molecular ions energies [1]. Fig. 3.1 illustrates the bandstructure of bilayer graphene calculated with DFT in ATK. The opening of a bandgap is clearly shown when a bias voltage of 8 V/nm is applied. DFT can also been used to study the channel scaling of nm-scale GFET, in which the devices consist of at most a few hundred carbon atoms and are costly for experimental exploration [11]. The modelled sub-10nm GFET exhibits a monotonic increase of intrinsic cut-off frequency from 3.4 to 21 THz while the gate length is scaled from 9.86 to 0.91 nm. Since the complexity of DFT increases as N^3 where N is the number of orbitals, it is necessary to include empirical model and fitting parameters to reduce the computing time in larger system simulations.
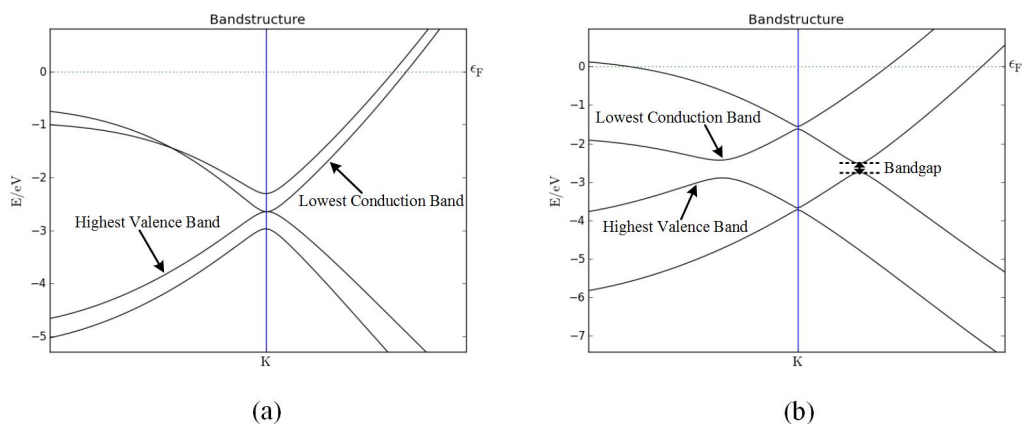
Figure 3.1: Bandstructure of bilayer graphene under vertical bias voltage (a) 0V/nm (b) 8 V/nm. Calculated with DFT in ATK [6].

3.1.2 Atomistic Modelling

The modelling of larger systems requires simplification to the DFT calculations. This can be achieved by defining an atomistic basis set for the Hamiltonian of the device material. Thus, the dispersion relation of DFT can be reproduced by utilizing a number of fitting parameters, greatly reducing the computational cost.

Extended Hückel theory [12] and SlaterKoster tight-binding scheme [13] are two well-known options for atomistic modelling. The later one has less number of orbitals which means less computing wall time but it cost more time to calculate the Hamiltonian elements. The atomistic modelling allows the performance simulation of larger and more complicated graphene devices with reasonable accuracy. As shown in Fig. 3.2, the bandstructure of bilayer graphene calculated with Extended Hückel Model in ATK is presented, in consistent with the calculation results of DFT in Fig. 3.1. The electronic transportation properties is achieved by solving nonequilibrium Greens function (NEGF) formalism with the results achieved from DFT or tight-binding (extended Hückel) method.
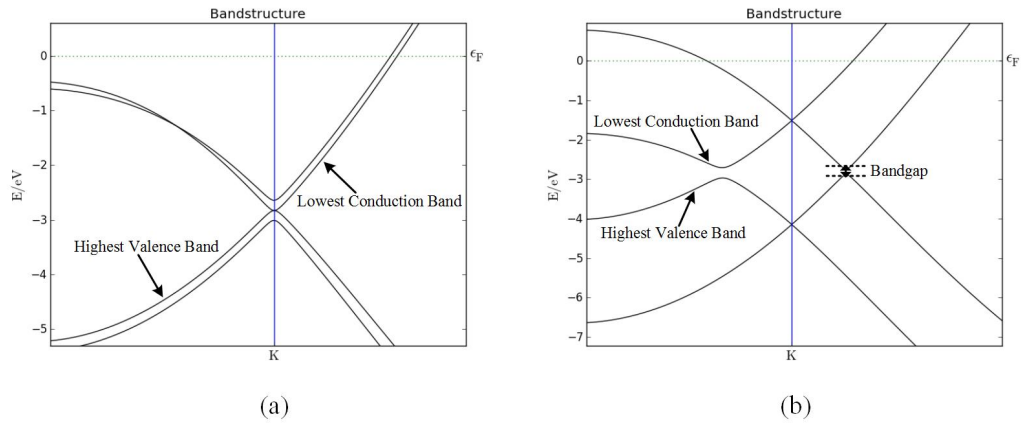
Figure 3.2: Bandstructure of bilayer graphene under vertical bias voltage (a) 0V/nm (b) 8 V/nm. Calculated with Extended Hückel Model in ATK [6].

3.1.3 Semiclassical Device Modelling

Semiclassical physical modelling tends to achieve accurate electrostatics characteristics and electronic transportation properties of large-scale devices. The empirical models and fitting parameters used in semiclassical modelling are extracted from measurement or reliable *ab initio*/atomistic calculations. The charge-voltage and current-voltage relations are achieved by solving the Poisson's equation and drift-diffusion model/Boltzmann transport equation, respectively.

The necessary parameters for semiclassical modelling are band structure, scattering rate/mobility and interband tunnelling rates [1]. In drift-diffusion model the fundamental physical parameter is the carrier mobility while in Boltzmann transport equation, the scattering rate is used. The early semiclassical drift-diffusion GFET model proposed by [14] successfully revealed the physical mechanisms behind the kink-like feature in the saturation current of GFETs. This was followed by a list of publications focused on theoretical studies [15, 16]. Although the current-voltage characteristics calculated from these models do not match very well with the measurement, they do provide physical insight that can be effectively used for device performance optimization.

3.1.4   Analytical Modelling

Compared with *ab initio* and atomistic modelling, the semiclassical models can reduce the computing time and achieve reasonable accuracy for large-scale device simulation if empirical models and fitting parameters are properly selected. However, the model proposed in [15, 16] need to be solved numerically, limiting its application for circuit analysis as commercial circuit simulators require analytical models with closed-form solutions. Recently, a series of GFET models fulfilling this requirement have been proposed [17–22]. These analytical models can be directly imported into commercial software such as Keysight ADS [23] for circuit analysis. Compared with the semiclassical model, reasonable approximations and/or empirical parameters have been implemented in these models to achieve closed-form expressions. In addition to that, a comprehensive model for hand-calculation was also presented in [24], allowing direct identification of dominant physical parameters in GFET design. Moreover, a Verilog-A compactible model was also proposed by [25], not only achieving improved accuracy in the vicinity of the charge neutrality (Dirac) point but also providing a compact model that can be directly used in circuit simulators.

3.2   Derivation of Analytical Closed-Form GFET Model

As introduced before, *ab initio* and atomistic modelling are suitable for device-level analysis of atomic-scale graphene transistors. To model large-scale graphene devices, a semiclassical modelling approach, with numerical solutions is needed, providing information for device parameters and geometry optimization. As for circuit analysis, the analytical modelling method with closed-form solutions that can be directly imported into commercial circuit simulators, is desired. Although existing analytical GFET models are in agreement with measurement data for either electron or hole conduction, modelling of both conduction modes simultaneously is inaccurate due to the use of identical carrier mobility for both electrons and holes. The mobility difference between electrons and

holes has been observed in many experiments [26–28]. This difference can sometimes be as high as 23 % [27]. Thus, using the same carrier mobility for electrons and holes would cause mismatching for either electron or hole conduction, depending on which mode the model is optimised for. Although there have been reports using distinct mobilities for each of the charge carriers [29–31], these models match poorly with measurement data. Moreover, it has been reported that carrier mobility decreases with the increase of carrier density in monolayer graphene [26, 28], but in all the GFET models mentioned so far a constant carrier mobility is used. Therefore, the model presented in this thesis aims to create an effective carrier mobility, taking into account the mobility difference in electron and hole, including the mobility variation against the carrier density.

3.2.1 Drift-Diffusion Transport Model of GFET

The schematic of a dual-gate GFET, with intrinsic region and external series resistances, is shown in Fig. 3.3. Assume the GFET channel is longer than the mean free path of graphene [32], the drift-diffusion transport theory is suitable for calculating the DC current of GFET [15]

$$I_{ds} = -Q_t v(x)W = -q\rho_{sh}(x)v(x)W, \tag{3.1}$$

where I_{ds} is the drain-to-source current, Q_t is the charge density in the channel, q the elementary charge. $\rho_{sh}(x)$ the the free carrier sheet density in the graphene channel at position x, $v(x)$ the carrier drift velocity at x and W is the channel width. It is noted although the model is based on drift-diffusion transport theory, the diffusion current is ignored in the modelling of GFET.

The model of carrier drift velocity in silicon has been well studied and the analytical
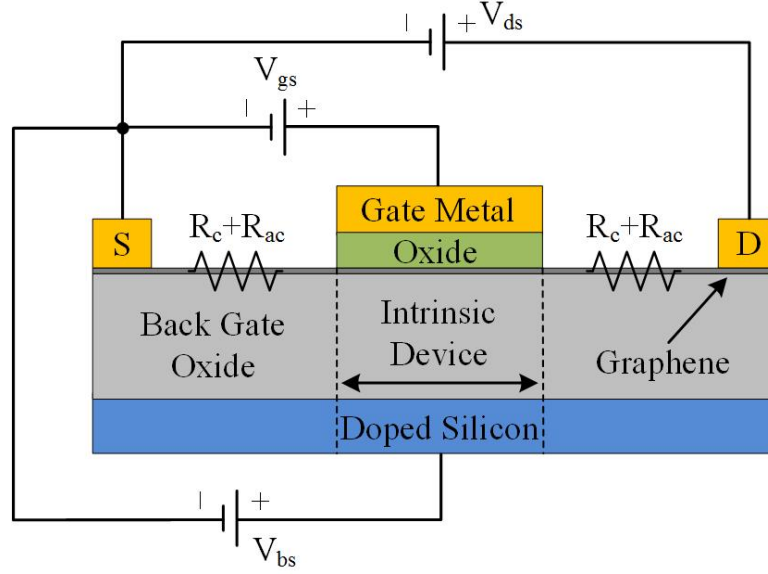
Figure 3.3: Cross section of dual-gate GFET modelled in this thesis. The channel material is monolayer graphene. Voltages V_{gs} and V_{bs} are top- and back-gate voltages. V_{ds} is the voltage between external drain (D) and source (S) electrodes. Contact and access resistances (R_c and R_{ac}) are considered as one resistance for both source and drain. Intrinsic device is the region covered by the top gate.

expression has been proposed as [33]

$$v = \frac{\mu E}{\left[1 + \left(\frac{\mu E}{V_{sat}} \right)^{\beta} \right]^{\frac{1}{\beta}}}, \tag{3.2}$$

where E is the electric field in the channel, μ the low-field carrier mobility, V_{sat} the saturation velocity and β is a fitting parameter. In [15] [17], a soft saturation model based on Eq. (3.2) has been proposed to model the drain current of GFET:

$$v = \frac{\mu E}{1 + \frac{\mu |E|}{V_{sat}}}. \tag{3.3}$$

The resulting drift velocity of Eq. (3.3) is in consistent with the Monte Carlo simulations of graphene velocity-field characteristics [34–36].

Meanwhile, the expression of electric field E can be written as

$$E = -\frac{dV(x)}{dx}, \tag{3.4}$$

where $V(x)$ is the local potential at position x. Thus, by substituting Eq. (3.3) and (3.4) into (3.1), the drain current can be rewritten as

$$I_{ds} = -q\rho_{sh}(x)\frac{\mu\left(-\dfrac{dV(x)}{dx}\right)}{1+\dfrac{\mu\left|-\dfrac{dV(x)}{dx}\right|}{V_{sat}}}W \tag{3.5}$$

By separating variables, Eq. (3.5) can be rearranged as

$$I_{ds}dx = -\frac{\mu I_{ds}}{V_{sat}}|dV(x)| + q\rho_{sh}\mu W dV(x) \tag{3.6}$$

Now if one integrate the left hand side of Eq. (3.6) over x from 0 to L (channel length) and the right hand side over $V(x)$ from 0 to V_{ds}:

$$\int_0^L I_{ds}dx = -\int_0^{V_{ds}}\frac{\mu I_{ds}}{V_{sat}}|dV(x)| + \int_0^{V_{ds}} q\rho_{sh}\mu W dV(x) \tag{3.7}$$

where V_{ds} is the drain-to-source voltage (V_d - V_s). When simplifed yields the final expression of drain current [25]

$$I_{ds} = W\frac{q\int_0^{V_{ds}}\mu\rho_{sh}dV}{L+\left|\int_0^{V_{ds}}\dfrac{\mu}{V_{sat}}dV\right|}. \tag{3.8}$$

It is worth mentioning that the voltages used here (i.e. V_d, V_s) are internal voltages applied on the intrinsic device. Meanwhile, the drift-diffusion transport model used in this thesis is valid only when the graphene channel is longer than the mean free path of carriers in graphene. If the channel length is close to or shorter than the mean free path, necessary short-channel effects have to be taken into account.

3.2.2   Aspects of GFET Modelling

In order to solve Eq. (3.8), it is important to introduce some important modelling aspects including effective carrier mobility, quantum capacitance, charge density and saturation velocity. As there are two integrals in it, in order to derive accurate closed-form analytical solutions the expressions of these aspects should match this criteria whilst retaining reasonable accuracy.

3.2.2.1   Charge Density in Graphene Channel

As we know, graphene is an atomically thick 2D material with zero bandgap. That means the top of its valance and the bottom of its conduction band overlaps with each other. The linear dispersion relation around the K point of the Brillouim zone, as depicted in Eq. (3.9), results in the well-known conical bandstructure of graphene near the Dirac point [37].

$$E(K) - E_{CV} = E(k) = \pm \hbar v_F |k_0| \tag{3.9}$$

Here, '+' is used for the conduction band and '-' for the valence band, E is the energy and E_{CV} is the energy at Dirac point, $\hbar$ the reduced Planck constant, v_F Fermi velocity (10^8 cm/s) and k_0 is the wave vector measured from the K point.

The number of available states in k space for a $A = L \times L$ real space graphene area can be expressed as

$$N = g_S g_V \frac{\pi k_0^2}{(2\pi/L)^2} = \frac{g_S g_V A k_0^2}{4\pi} = \frac{g_S g_V A}{4\pi} \left(\frac{E - E_{CV}}{\hbar v_F} \right)^2 \tag{3.10}$$

where g_S and g_V are the degeneracy factors of spin and valley respectively. Utilizing $g_S g_V = 4$ [15], the DoS in graphene can be derived as

$$D(E) = \frac{1}{A} \frac{dN}{dE} = \frac{2}{\pi} \frac{|E - E_{CV}|}{(\hbar v_F)^2} \tag{3.11}$$

Taking the Fermi-Dirac probability function

$$f(E) = \frac{1}{\exp\left(\dfrac{E - E_F}{kT}\right) + 1} \tag{3.12}$$

as the probability of occupied states, where k is the Boltzmann constant, T the temperature and E_F the Fermi level, the electron density can be easily achieved as the integral of the product of $D(E)$ and $f(E)$ from E_{CV} to ∞:

$$n = \int_{E_{CV}}^{\infty} D(E)f(E)dE \tag{3.13}$$

Substituting the analytical expressions of $D(E)$ and $f(E)$ given in Eq. (3.11) and (3.12) into (3.13), the electron sheet density can be rewritten as

$$n = \int_{E_{CV}}^{\infty} \frac{2}{\pi} \frac{|E - E_{CV}|}{(\hbar v_F)^2} \frac{1}{\exp\left(\dfrac{E - E_F}{kT}\right) + 1} dE \tag{3.14}$$

Substituting $E' = E - E_{CV}$ and $E_F - E_{CV} = qV_{ch}$ to Eq. (3.14), the following expression of electron sheet density can be achieved

$$n = \frac{2}{\pi (\hbar v_F)^2} \int_0^{\infty} \frac{E'}{\exp\left(\dfrac{E' + E_{CV} - E_F}{kT}\right) + 1} dE'$$

$$= \frac{2}{\pi (\hbar v_F)^2} \int_0^{\infty} \frac{E'}{\exp\left(\dfrac{E' - qV_{ch}}{kT}\right) + 1} dE' \tag{3.15}$$

where V_{ch} is the channel potential.

Similarly, the expression of hole sheet density can be achieved as

$$p = \frac{2}{\pi (\hbar v_F)^2} \int_0^{\infty} \frac{E'}{\exp\left(\dfrac{E' + qV_{ch}}{kT}\right) + 1} dE'. \tag{3.16}$$

The analytical expression of Eq. (3.15) and (3.16) are approximated as [15]

$$n = \frac{2(kT)^2}{\pi(\hbar v_F)^2} \mathfrak{F}_1\left(\frac{-qV_{ch}}{kT}\right) \tag{3.17}$$

$$p = \frac{2(kT)^2}{\pi(\hbar v_F)^2} \mathfrak{F}_1\left(\frac{qV_{ch}}{kT}\right) \tag{3.18}$$

where $\mathfrak{F}_1(\cdot)$ is the Fermi-Dirac integral of first order and the expression of short series approximation of $\mathfrak{F}_1(\cdot)$ is given as [38] [39]

$$\mathfrak{F}_1\left(\frac{qV_{ch}}{kT}\right) = \begin{cases} \sum_{i=1}^{7} a_i e^{i \cdot V_{ch}}, & \text{if } V_{ch} \leqslant 0 \\ \sum_{i=1}^{7} (-1)^i a_i e^{i \cdot V_{ch}} + b_1 + b_2 \cdot V_{ch}^2, & \text{if } V_{ch} > 0 \end{cases} \tag{3.19}$$

where $a_1 = 1.000000$, $a_2 = 0.250052$, $a_3 = 0.111747$, $a_4 = 0.064557$, $a_5 = 0.040754$, $a_6 = 0.020532$, $a_7 = 0.005108$, $b_1 = 1.644934066848226$, and $b_2 = 0.500000000000000$ are fitting parameters. The relative error of Eq. (3.19) is on the level of 10^{-6}. Thus, the total net mobile sheet charge density (assume hole conduction)

$$Q_{net} = q \times (p - n) = \frac{2q(kT)^2}{\pi(\hbar v_F)^2} \left(\mathfrak{F}_1\left(\frac{qV_{ch}}{kT}\right) - \mathfrak{F}_1\left(\frac{-qV_{ch}}{kT}\right)\right) \tag{3.20}$$

Q_{net} is used to derive the expression of quantum capacitance and sometimes is also used instead of the charge density relevant for transport

$$Q_t = q \times (p + n) = \frac{2q(kT)^2}{\pi(\hbar v_F)^2} \left(\mathfrak{F}_1\left(\frac{qV_{ch}}{kT}\right) + \mathfrak{F}_1\left(\frac{-qV_{ch}}{kT}\right)\right) \tag{3.21}$$

in the calculation of drain current [15] [19] [17] [21]. Fig. 3.4 depicts the plot of Q_{net} and Q_t as a function of V_{ch}. It is easy to see that Q_{net} differs from Q_t near $V_{ch} = 0$. Q_{net} equals to zero at $V_{ch} = 0$ while Q_t reaches a non-zero low carrier density. Apparently, the carrier density relevant for transport at the Dirac point is not zero. Utilizing Q_t rather than Q_{net} in drain current calculation is able to improve the accuracy of GFET models since all the free carriers in the channel would contribute to the overall drain current. In order to derive closed-form solutions for drain current calculation, a simplified expression
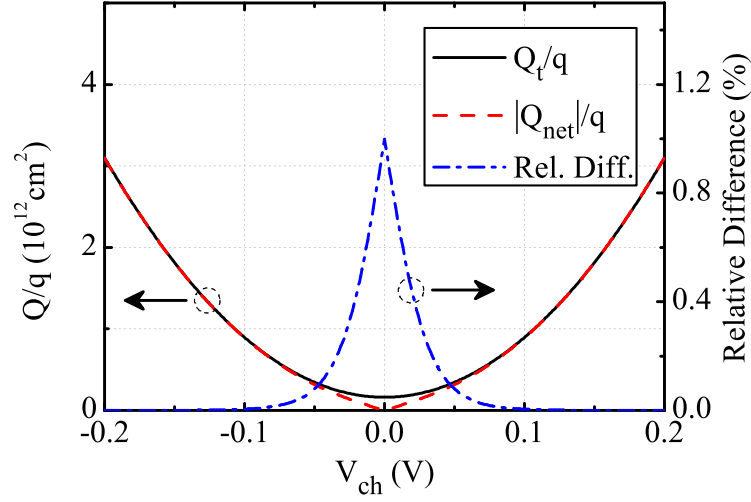
Figure 3.4: Charge density as a function of the channel potential V_{ch} (left axis): Q_{net} and Q_t. The relative difference (right axis) is also shown.

of Q_t used in [18] with good agreement with Eq. (3.21) is used in this work

$$Q_t = \frac{q\pi(kT)^2}{3(\hbar v_F)^2} + \frac{q^3 V_{ch}^2}{\pi(\hbar v_F)^2}$$ (3.22)

The relative difference between Eq. (3.21) and (3.22) is on the level of 10^{-6}.

Except Q_t, another important fraction of channel charge density should be taken into account is the residual charge due to electron-hole puddles [26]

$$n_{pud} = \frac{\Delta^2}{\pi(\hbar v_F)^2},$$ (3.23)

It is caused by the intrinsic ripples in graphene and extrinsic charge-induced inhomogeneities in the carrier density and Δ is the inhomogeneity of the electrostatic potential. Thus, the total transport sheet carrier density can be written as

$$Q_{tot} = q\rho_{sh} = Q_t + q n_{pud}$$ (3.24)

3.2.2.2 Quantum Capacitance

The theory of quantum capacitance for devices with two-dimensional electron gas (2DEG) has been discussed in details in [40]. As we know, the grounded metal plate is able to fully shield the quasistatic electric fields. That means the electric fields emitted from charges on one side of the grounded metal plate cannot penetrate into the other side. Therefore, the capacitance seen at the node 1 of a three-plate system, as shown in Fig. 3.5(a), can be easily calculated using the expression of a parallel-plate capacitor

$$C = C_1 = \epsilon_1 \epsilon_0 \frac{A}{d_1} \tag{3.25}$$

where ϵ_1 is the relative permittivity of the dielectric between the parallel plates, ϵ_0 is the vacuum permittivity, A is the area of overlap of the plates (m^2) and d_1 is the distance between the plates.

If the middle plate is made of 2DEG rather than metal, the electric filed would partially penetrate through it and induce charges on the bottom plate. Thus, the expression of Eq. (3.25) is not valid for the capacitance seen at node 1 any more. The equivalent circuit of the total capacitance for the new system should be depicted as Fig. 3.5(b), where $C_q = \dfrac{g_V m q^2}{\pi \hbar^2}$ is called quantum capacitance [40]. g_V is factor of the valley degeneracy, m is the effective mass of electron. When the middle plate is metal, $C_q = 0$ and $C = C_1$. When the middle plate is 2DEG, $C = \dfrac{C_1 C_q}{C_1 + C_q}$. C_q is resulted from the Pauli principle which requires additional energy to fill the 2DEG with electrons. The concept of quantum capacitance has been widely used in the modelling of devices with 2DEG [41] and has also been extended to the modelling of one-dimensional carbon nanotube device [42].

In the modelling of GFET, due to the finite DoS in graphene, one should also take the effects of quantum capacitance into consider. Fig. 3.6(a) depicts the effective gate
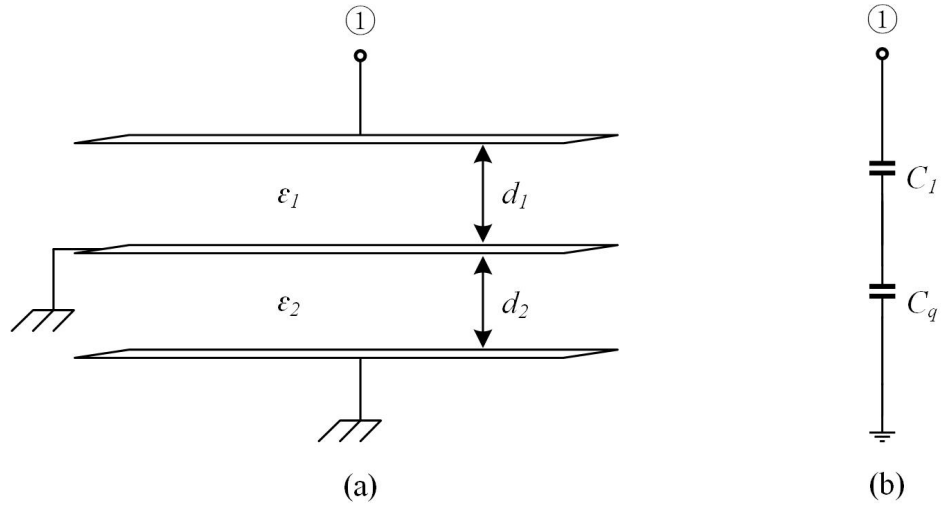
Figure 3.5: (a) Schematic of the three-plate capacitor. (b) Equivalent circuit for the capacitance seen at node 1 when the middle plate is graphene or 2D electron gas.
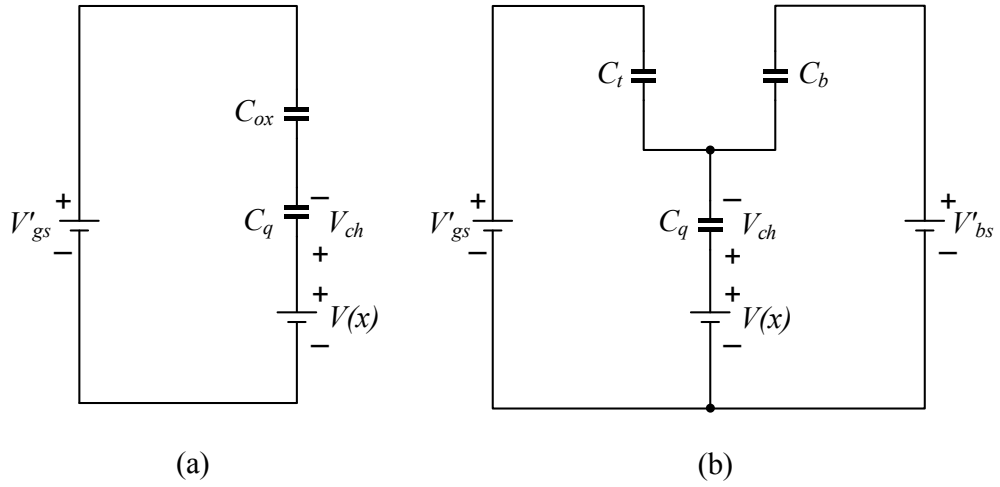
Figure 3.6: Equivalent circuit of GFET gate electrostatics describing the relationship between gate oxide capacitances (C_{ox}, C_t and C_b) and quantum capacitance C_q (a) single gate (b) dual gate. V'_{gs} and V'_{bs} are the net top- and back-gate voltage respectively. V_{ch} represents the channel potential and $V(x)$ refers to the voltage drop in the channel.

capacitance C_g of a single gate GFET

$$C_g = \frac{C_q C_{ox}}{(C_q + C_{ox})} \tag{3.26}$$

where C_{ox} is the gate oxide capacitance. The quantum capacitance of GFET is defined as [37]

$$C_q = -\frac{dQ_{net}}{dV_{ch}} \tag{3.27}$$

where V_{ch} is called channel potential that defined as the voltage across C_q. The exact expression of C_q has been derived as [37]

$$C_q = \frac{2q^2 kT}{\pi (\hbar v_F)^2} \ln\left[2\left(1 + \cosh\left(\frac{qV_{ch}}{kT}\right)\right)\right]. \tag{3.28}$$

As our goal is to derive a closed-form analytical solution for the drain current, the expression in Eq. (3.28) is too complicated for this purpose. Hence, in [14–17] the C_q is approximated as

$$C_q = \frac{2q^2}{\pi} \frac{q|V_{ch}|}{(\hbar v_F)^2}. \tag{3.29}$$

where the quantum capacitance is positively proportional to the channel potential (i.e. $C_q \propto |V_{ch}|$). It has been pointed out in [25] this approximation is not accurate near the Dirac point. In order to achieve more accurate modelling results, they proposed a square-root approximation, which is in consistent with the exact model given in Eq. (3.28) and able to provide closed-form solution to the drain current

$$C_q = \frac{2q^2 kT \ln(4)}{\pi (\hbar v_F)^2} \sqrt{1 + \left(\frac{qV_{ch}}{kT \ln(4)}\right)^2}. \tag{3.30}$$

The comparison between three C_q models are shown in Fig. 3.7. It is clearly seen that the model in Eq. (3.29) differs from the other two models at low V_c and the square-root approximation agrees well with the exact model, with a maximum relative difference of 8%.
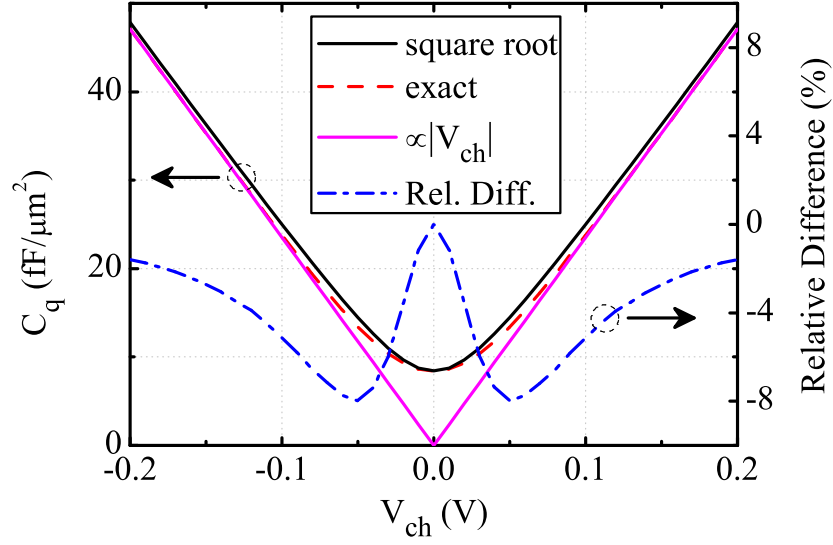
Figure 3.7: Quantum capacitance as a function of the channel potential V_{ch} (left axis): square-root, exact and $\propto |V_{ch}|$ models. The relative difference (right axis) between the square-root and exact models is also shown.

3.2.2.3 Effective Carrier Mobility

The carrier mobility describes how fast carriers can move through the graphene channel under certain electric field. Distinct mobility for holes and electrons has been observed experimentally in graphene [26] [27] [28]. The relation between mobility and carrier density has been studied in [26] through experiments and modelling. It is found that in monolayer graphene the mobility tends to decrease when the carrier density increases, as shown in Fig. 3.8(a). In contrast, for bi-layer and tri-layer graphene the mobility rises as the carrier density increases, as shown in Fig. 3.8(b) and (c). In addition, mono- and multilayer graphene also exhibit opposite temperature dependence, as shown in Fig. 3.8.

In order to explore the mechanism behind the temperature and carrier density dependent mobility of mono- and multilayer graphene, the expression of carrier mobility for monolayer has been approximated as [26]

$$\mu_{mono}^{-1} \approx \mu_{C\_mono}^{-1} + \mu_{sr\_mono}^{-1} + \mu_{gr\_mono}^{-1} + \mu_{ox\_mono}^{-1} \tag{3.31}$$
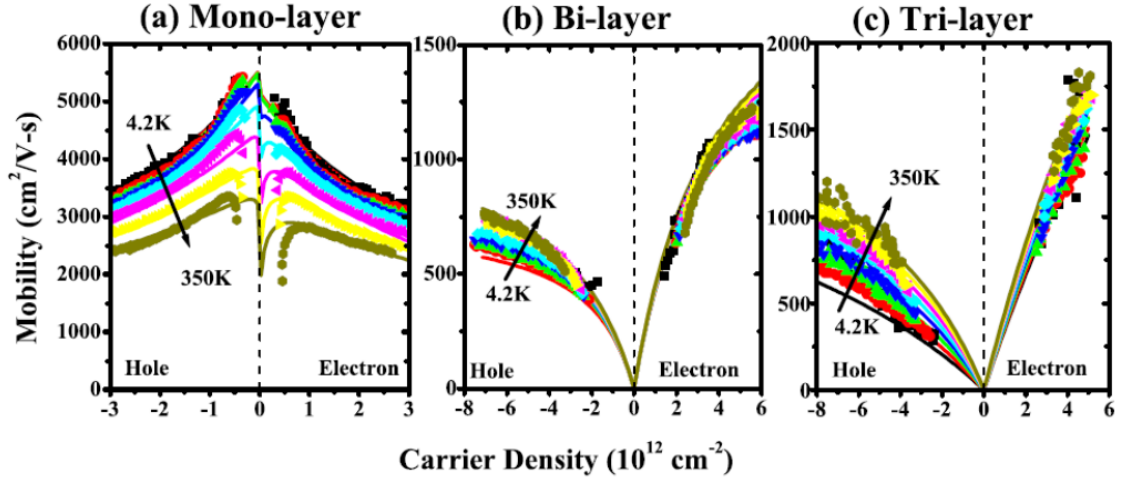
Figure 3.8: Measured mobility vs. carrier density at various temperature (a) Monolayer graphene. (b) bilayer graphene. (c) trilayer graphene [26].

where

$$\mu_{C\_mono} = S_C \tag{3.32}$$

and

$$\mu_{sr\_mono} = \frac{S_{sr}}{\rho} \tag{3.33}$$

are the mobility limited by the Coulomb and short-range scattering, respectively. ρ is the carrier density. S_C and S_{sr} are fitting parameters.

$$\mu_{gr\_mono} = \frac{S_{gr}}{\rho T} \tag{3.34}$$

and

$$\mu_{ox\_mono} = S_{ox}\rho^\gamma \left(\frac{1}{\exp\left(\dfrac{59\,\text{meV}}{kT}\right) - 1} + \frac{6.5}{\exp\left(\dfrac{155\,\text{meV}}{kT}\right) - 1} \right)^{-1} \tag{3.35}$$

are the mobility limited by graphene acoustic phonon and substrate (e.g. SiO$_2$) surface polar phonon scattering, respectively. S_{gr}, S_{ox} and γ are fitting parameters. It is easy

to see μ_{sr_mono} and μ_{gr_mono} decrease with the increase of ρ, resulting in the decreasing carrier mobility. On the other hand, when the temperature increases μ_{gr_mono} and μ_{ox_mono} decrease, resulting in the decreasing carrier mobility.

In multilayered graphene, the situation is different that the phonon scatterings (i.e. the mechanisms behind μ_{gr_multi} and μ_{ox_multi}) are screened by the extra graphene layers [43, 44]. Hence, the the Coulomb and short-range scattering dominate in the resulting carrier mobility. Therefore, the mobility of multilayer graphene can be written as [26]

$$\mu_{multi}^{-1} \approx \mu_{C\_multi}^{-1} + \mu_{sr\_multi}^{-1} \tag{3.36}$$

where

$$\mu_{C\_multi} = (A + BT)\rho \tag{3.37}$$

and

$$\mu_{sr\_multi} = C \tag{3.38}$$

are the Coulomb and short-range scattering limited mobility of multilayer graphene, respectively. A, B and C are fitting parameters. Thus, it is easy to see the mobility of multilayer graphene is positively proportional to the temperature and carrier density.

Hence, a good room-temperature GFET model should not only take into account the hole electron mobility difference but also include a carrier density dependent mobility. Since the GFET to be modelled utilises monolayer graphene, the mobility should decrease with the increase of the carrier density. Assume the low field mobilities of electron and hole are μ_n and μ_p respectively and ignore the temperature effects, the effective carrier mobility is defined as

$$\mu_{eff} = \frac{n \cdot \mu_n + p \cdot \mu_p + n_{pud} \cdot h}{n + p + n_{pud}}. \tag{3.39}$$

where $h = (\mu_n + \mu_p)/2$. From the expression derived for n and p in Eq. (3.17) and Eq. (3.18), the effective carrier mobility can be expressed as a function of the channel potential V_{ch}. Fig. 3.9 illustrates μ_{eff} as a function of V_{ch}. It is clearly shown that
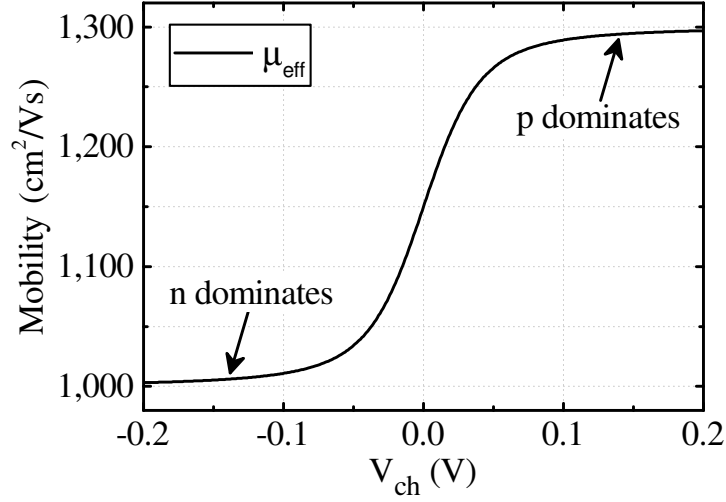
Figure 3.9: μ_{eff} as a function of the channel potential V_{ch}. Parameters used in this graph: $\mu_n = 1000\,\text{cm}^2/\text{Vs}$, $\mu_p = 1300\,\text{cm}^2/\text{Vs}$ and $\Delta = 30\,\text{meV}$.

in n (or p) dominant region, μ_{eff} coincides with n (or p). Since the carrier mobility of monolayer graphene decreases with the increase of carrier density, an empirical model ignoring the temperature effects has been proposed as [28]

$$\mu'_{eff} = \frac{\mu_{eff}}{1 + \left(\dfrac{Q_t}{Q_{ref}}\right)^{\beta}}, \tag{3.40}$$

where the reference carrier density Q_{ref} and β are fitting parameters. Although Eq. (3.40) provides good fitting for mobility vs. carrier density, it dose not satisfy the requirement of closed-form analytical solution. Therefore, in this work the following simplifications has to be made. Firstly, when $q|V_{ch}| \gg kT$ and $q|V_{ref}| \gg kT$ one can achieve the following approximation from Eq. (3.22) as

$$\frac{Q_t}{Q_{ref}} = \frac{\dfrac{q\pi(kT)^2}{3(\hbar v_F)^2} + \dfrac{q^3 V_{ch}^2}{\pi(\hbar v_F)^2}}{\dfrac{q\pi(kT)^2}{3(\hbar v_F)^2} + \dfrac{q^3 V_{ref}^2}{\pi(\hbar v_F)^2}} \approx \frac{V_{ch}^2}{V_{ref}^2}, \tag{3.41}$$

where V_{ref} is the reference channel potential. Secondly, since β is the secondary fitting parameter which plays a less important role compare with Q_{ref}, it is set to 1 in order to

simplify the model of effect carrier mobility. Thus, Eq. (3.40) can be rewritten as

$$\mu'_{eff} = \frac{\mu_{eff}}{1 + \left(\frac{V_{ch}^2}{V_{ref}^2}\right)^1} = \frac{n \cdot \mu_n + p \cdot \mu_p + n_{pud} \cdot h}{n + p + n_{pud}} \left(\frac{m}{m + V_{ch}^2}\right), \tag{3.42}$$

where $m = V_{ref}^2$. Unfortunately, Eq. (3.42) is still too complicated and does not result in closed-form analytical solutions. Therefore, an approximate mobility function μ_{pn} for carriers excluding n_{pud} (i.e. for $(n + p)$ only) is proposed

$$\mu_{pn} = \left(h + \frac{14zV_{ch}}{\sqrt{1 + \left(\frac{qV_{ch}}{(kT\ln(4))}\right)^2}}\right)\left(\frac{m}{m + V_{ch}^2}\right), \tag{3.43}$$

where $z = (\mu_p - \mu_n)$. Eq. (3.43) allows calculating the contributions of $(n + p)$ and n_{pud} to the drain current individually and enables analytical solutions for the drain current

$$\mu''_{eff} = \frac{(n + p) \cdot \mu_{pn} + n_{pud} \cdot h \cdot \left(\frac{m}{m + V_{ch}^2}\right)}{n + p + n_{pud}}. \tag{3.44}$$

Substituting Eq. (3.22) into (3.44), the final expression of the effective carrier mobility becomes

$$\mu''_{eff} = \frac{\frac{Q_t}{q} \cdot \mu_{pn} + n_{pud} \cdot h \cdot \left(\frac{m}{m + V_{ch}^2}\right)}{\frac{Q_t}{q} + n_{pud}}$$

$$= \frac{\left(a + bV_{ch}^2\right) \cdot \left(h + \frac{14 \cdot z \cdot V_{ch}}{\sqrt{1 + cV_{ch}^2}}\right) + n_{pud} \cdot h}{\left(a + bV_{ch}^2\right) + n_{pud}} \cdot \left(\frac{m}{m + V_{ch}^2}\right)$$

$$= \frac{\left(a + bV_{ch}^2 + n_{pud}\right) \cdot h + \left(a + bV_{ch}^2\right) \cdot \frac{14 \cdot z \cdot V_{ch}}{\sqrt{1 + cV_{ch}^2}}}{a + bV_{ch}^2 + n_{pud}} \cdot \left(\frac{m}{m + V_{ch}^2}\right)$$

$$= \left(\frac{14 \cdot z \cdot (a + bV_{ch}^2)}{(a + bV_{ch}^2 + n_{pud})} \cdot \frac{V_{ch}}{\sqrt{1 + cV_{ch}^2}} + h \right) \left(\frac{m}{m + V_{ch}^2} \right). \tag{3.45}$$

Here, $a = \pi(kT)^2/(3(\hbar v_F)^2)$, $b = q^2/(\pi(\hbar v_F)^2)$ and $c = q^2/((kT \ln(4))^2$. In Fig. 3.10, Eq. (3.42) and (3.45) are plotted as well as the relative difference defined as $(\mu'_{eff} - \mu''_{eff})/\mu'_{eff} \times 100\%$. It can be seen that μ'_{eff} and μ''_{eff} match very well and the maximum relative difference is about $\pm 1.5\%$ only in this example.

3.2.2.4 Saturation Velocity

Saturation velocity is the maximum drift velocity a carrier in graphene reaches under high electric fields. Both Monte Carlo simulation and experimental results have shown velocity saturation on the order of $10^5 \sim 10^6$ m/s in graphene [28] [36]. V_{sat} is an important parameter and has been modelled as inversely proportional to the channel potential ($\propto |V_{ch}^{-1}|$) in [17] [20]. This $\propto |V_{ch}^{-1}|$ approximation provides accurate V_{sat} at high V_{ch} but at low V_{ch} it gives unrealistic results (i.e. infinite V_{sat}) [25]. Therefore, a two-region model was proposed as [16]

$$\rho_{crit} = \frac{1}{2\pi} \left(\frac{\Omega}{v_F} \right)^2, \tag{3.46}$$

$$V_{sat} = \begin{cases} \dfrac{2v_F}{\pi}, & \text{if } |Q_{net}| \leqslant q|\rho_{crit}| \\ \dfrac{2q\Omega}{\pi^2 \hbar v_F |Q_{net}|} \cdot \sqrt{\dfrac{\pi \left(\hbar v_F{}^2 \right) |Q_{net}|}{q} - \left(\dfrac{\hbar\Omega}{2} \right)^2}, & \text{if } |Q_{net}| \geqslant q|\rho_{crit}| \end{cases} \tag{3.47}$$

where Ω is a factor along with $\hbar$ to represent the effective optical phonon emitting energy ($\hbar\Omega$). Eq. (3.47) agrees well with the $\propto |V_{ch}^{-1}|$ model at high V_{ch}. At low V_{ch}, instead of letting the saturation velocity increase to infinite, the two-region model forces V_{sat} to be a constant value when the charge density Q_{net} is smaller than the predefined factor ρ_{cri}. Thus, the saturation velocity becomes constant around the Dirac point and this model has also been designed to preserve continuous V_{sat} at ρ_{cri}. The comparison of using $\propto |V_{ch}^{-1}|$ and the two-region model for saturation velocity have also been discussed
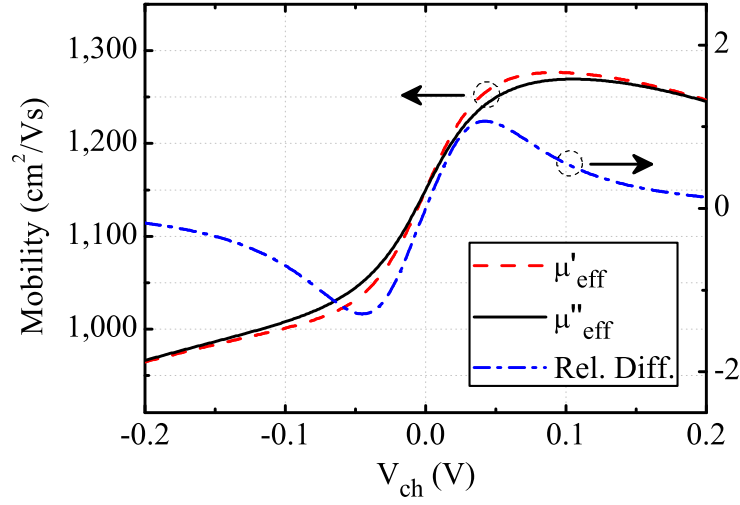
Figure 3.10: Effective carrier mobility as a function of the channel potential V_{ch} (left axis): exact model μ'_{eff} and approximation μ''_{eff}. The relative difference (right axis) is also shown. Parameters used in this graph: $\mu_n = 1000\,\text{cm}^2/\text{Vs}$, $\mu_p = 1300\,\text{cm}^2/\text{Vs}$, $m = 1\,V^2$, $\Delta = 30\,\text{meV}$.

in [25].

In spite of the benefits introduced in the previous paragraph, the two-region model has disadvantages. Primarily the observed discontinuities in the calculated transconductance g_m, and it becomes even more apparent for higher carrier mobility. This occurs due to the sudden change of saturation velocity function at ρ_{cri}. Although the V_{sat} is designed to be continuous at ρ_{cri}, it does not guarantee the continuity of g_m calculated as dI_{ds}/dV_{gs}. Meanwhile, the two-region model does not satisfy the requirement of deriving closed-form drain current solutions with Eq. (3.45). Therefore, in this work we propose another approximation for V_{sat} as

$$V_{sat} = v_F \left(\frac{e}{1 + fV_{ch}^2} + g \right), \tag{3.48}$$

where $e = (V_{sat}(\text{max}) - V_{sat}(\text{min}))/v_F$, $f = (q/(5kT))^2$ and $g = V_{sat}(\text{min})/v_F$. From the two-region model, the values of $e = 0.58$ and $g = 0.058$ can be extracted. The V_{sat} given by Eq. (3.48) consists of only one function so that the discontinuities in calculated g_m are eliminated. In addition, Eq. (3.48) can also be used with Eq. (3.45) to derive closed-form drain current solutions. Fig. 3.11 shows the plots of Eq. (3.47) and (3.48).
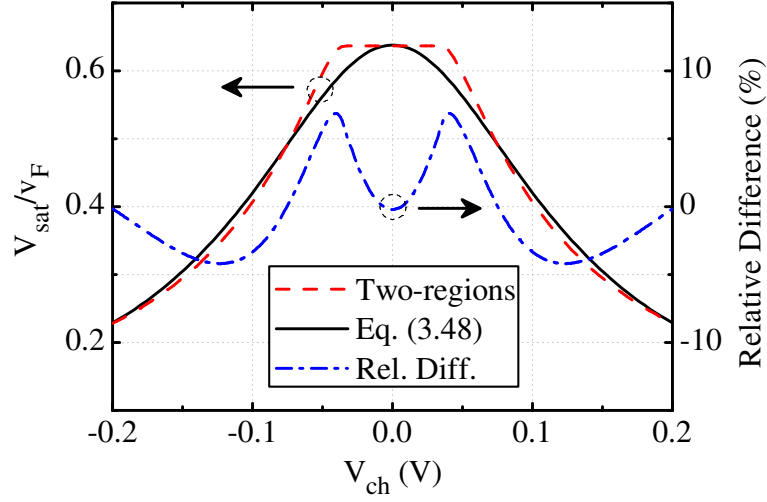
Figure 3.11: Ratio of saturation velocity V_{sat} to Fermi velocity v_F in graphene as a function of the channel potential V_{ch} (left axis): two-region model [16] and the proposed approximation. The relative difference (right axis) is also shown.

A relative difference $((V_{two-region} - V_{sat})/V_{two-region} \times 100\%)$ within $\pm 7\%$ guarantees the accuracy of the proposed V_{sat} model.

3.2.3 Closed-Form Drain Current Expression

This section describes the electrostatics and electronic transport calculation of the proposed analytical model. With the modelling aspects introduced in the last section, the closed-form solution of drain current is derived.

3.2.3.1 Electrostatics

The electrostatics of a dual-gate GFET is conducted with the equivalent circuit model illustrated in Fig. 3.6(b). The expression of channel potential can be derived by applying Kirchhoff's laws to the circuit as [25]

$$Q_{top} = [V_{gs} - V_{gs0} - V(x) + V_{ch}] C_t, \tag{3.49}$$

$$Q_{bot} = [V_{bs} - V_{bs0} - V(x) + V_{ch}] C_b, \tag{3.50}$$

$$Q_{net} = \alpha(V_{ch}) C_q V_{ch}, \tag{3.51}$$

where Q_{top} and Q_{bot} are the charges stored in C_t and C_b, respectively. V_{gs} and V_{bs} are the top- and back-gate voltages. V_{gs0} and V_{bs0} are the top- and back-gate voltages at which the drain current reaches minimum. $V(x)$ is the voltage drop in the graphene channel at x. C_t and C_b are the top- and back-gate oxide capacitances respectively. $\alpha(V_{ch})$ is the capacitance weighting factor defined as [25]

$$\alpha(V_{ch}) = \frac{Q_{net}}{C_q V_{ch}} = \frac{kT}{qV_{ch}} \frac{\mathfrak{F}_1\left(\frac{qV_{ch}}{kT}\right) - \mathfrak{F}_1\left(\frac{-qV_{ch}}{kT}\right)}{\ln\left[2\left(1 + \cosh\left(\frac{qV_{ch}}{kT}\right)\right)\right]}. \tag{3.52}$$

Since the system is charge neutral, we have

$$Q_{net} = -(Q_{top} + Q_{bot}) \tag{3.53}$$

Substituting Eq. (3.49) (3.50) and (3.51) into (3.53), the expression of V_{ch} can be achieved

$$V_{ch} = -\frac{(V_{gs} - V_{gs0} - V(x))C_t + (V_{bs} - V_{bs0} - V(x))C_b}{C_t + C_b + \alpha(V_{ch})C_q}. \tag{3.54}$$

From the exact model of α given in Eq. (3.52), one can achieve $\alpha \approx 1$ when $q \times |V_{ch}| \ll kT$ and $\alpha \approx 0.5$ when $q \times |V_{ch}| \gg kT$ (see the red dashed line in Fig. 3.12). So far, in order to achieve closed-form analytical solution to the drain current, many existing GFET models use a constant $\alpha = 0.5$ for Eq. (3.54), achieving poor accuracy near the Dirac point [25]. In the case of $\alpha = 1$, an overestimation would be introduced to the calculated drain current away from the Dirac point. Therefore, an accurate model should contain a transition from $\alpha = 1$ at $q \times |V_{ch}| \ll kT$ to $\alpha = 0.5$ at $q \times |V_{ch}| \gg kT$. In this work a new model α' providing closed-form analytical solutions to Eq. (3.8) is
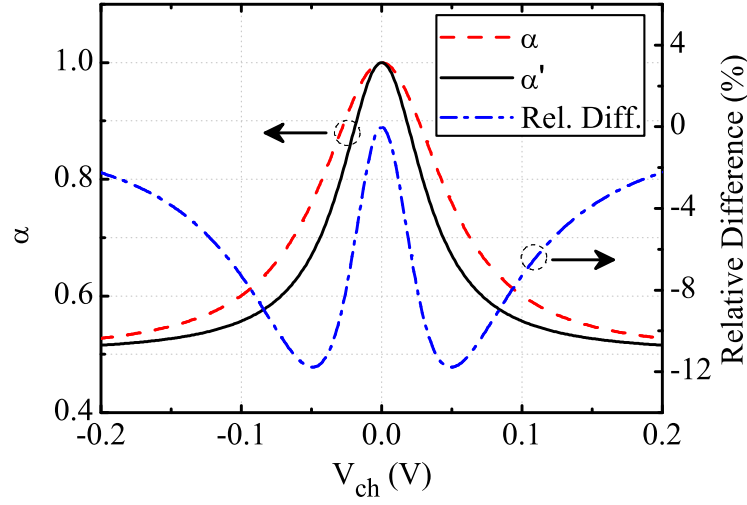
Figure 3.12: Capacitance weighting factor as a function of the channel potential V_{ch} (left axis): exact model α and approximation α'. The relative difference (right axis) is also shown.

proposed. It is an approximation of Eq. (3.52) and is given as a function of V_{ch}

$$\alpha'(V_{ch}) = \left(\frac{1}{1 + cV_{ch}^2} + 1 \right) \alpha_{min}, \qquad (3.55)$$

where $\alpha_{min} = 0.5$ is the minimum value of α. In Fig. 3.12, a comparison of α and α' are shown. A maximum relative difference $((\alpha - \alpha')/\alpha \times 100\,\%)$ of -12 % is achieved, guaranteeing the accurate transition between $\alpha = 0.5$ and $\alpha = 1$ near the Dirac point. This is a big improvement compared with the models using constant α.

Finally, to achieve V_{ch} and C_q, Eq. (3.28) and (3.54) should be solved self-consistently. The iterative Verilog-A algorithm, initially used in carbon nanotube FET models [45], has been successfully extended by Landauer et al. [25] to solve self-consistent equations in GFET modelling. Thus, it allows the simulator to find the solution of Eq. (3.54) automatically, greatly simplifying the calculation work. Fig. 3.13(a) and (b) are the equivalent circuits used in the Verilog-A algorithm. The aim is to calculate the channel potential at source and drain (i.e. V_{cs} and V_{cd}). Take the drain side as an example, the first step is to rewrite Eq. (3.54) as left-hand side (LHS) and right-hand side (RHS) terms:
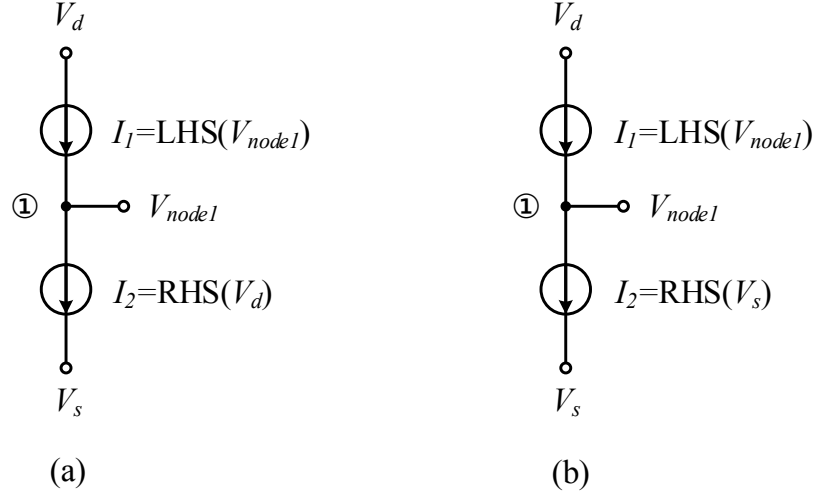
Figure 3.13: Equivalent circuits used to extract (a) V_{cd} and (b) V_{cs}.

$$\overbrace{(C_t + C_b + \alpha(V_{ch})C_q)V_{ch}}^{\text{LHS}} = \overbrace{-[(V_{gs} - V_{gs0} - V(x))C_t + (V_{bs} - V_{bs0} - V(x))C_b]}^{\text{RHS}}, \quad (3.56)$$

In the citcuit shown in Fig. 3.13(a), the following expressions of I_1 and I_2 are defined

$$
\begin{aligned}
I_1 &= \text{LHS}(V_{node1}) \\
&= (C_t + C_b)V_{node1} + \alpha(V_{node1})C_q(V_{node1})V_{node1} \\
&= (C_t + C_b)V_{node1} + Q_{net}(V_{node1}),
\end{aligned}
\quad (3.57)
$$

$$
\begin{aligned}
I_2 &= \text{RHS}(V_d) \\
&= -(V_{gs} - V_{gs0} - V_d)C_t - (V_{bs} - V_{bs0} - V_d)C_b,
\end{aligned}
\quad (3.58)
$$

where V_d is the voltage applied on the drain. During the simulation, the simulator would automatically force $I_1 = I_2$, hence we have

$$I_1 = \text{LHS}(V_{node1}) = \text{RHS}(V_d) = I_2 \quad (3.59)$$

Apparently, the voltage V_{node1}, that can be directly read out by the simulator from node 1, is the solution to Eq. (3.56) (i.e. V_{cd}). Similarly, V_{cs} can also be found with the circuit

shown in Fig. 3.13(b). During this process the elementary mathematical approximation of first order Fermi-Dirac integral given in Eq. (3.19) is used for Q_{net}.

3.2.3.2 Drain Current Calculation

The drift-diffusion model derived in Eq. (3.8) is used along with the modelling aspects introduced in Section 3.2.2 to calculate the drain current. Deriving closed-form analytical solution for the integrals in Eq. (3.8) requires replacing dV with $\dfrac{dV}{dV_{ch}}dV_{ch}$. To derive the closed-form solution for I_{ds}, the square-root approximation of C_q (i.e. Eq. 3.30) is used here. The expression of $\dfrac{dV}{dV_{ch}}$ is derived by substituting Eq. (3.30) and (3.55) into (3.54), taking the partial derivative of V against V_{ch} on both sides of the equation. When simplified yields,

$$\frac{dV}{dV_{ch}} = 1 + \frac{ds\left(2 + cV_{ch}^2\left(3 + 2cV_{ch}^2\right)\right)}{\left(1 + cV_{ch}^2\right)^{\frac{3}{2}}}.$$

(3.60)

Finally by substituting Eq. (3.22), (3.23), (3.24), (3.43) and (3.60) into (3.8) and assuming the effective channel potential to be $(V_{cs} + V_{cd})/2$ for n_{pud}, the numerator integral of Eq. (3.8) can be rewritten as

$$\int_{V_{cs}}^{V_{cd}} q\left(a + bV_{ch}^2\right)\left(h + \frac{14zV_{ch}}{\sqrt{1 + cV_{ch}^2}}\right)\left(1 + \frac{d\alpha_{min}\left(2 + cV_{ch}^2\left(3 + 2cV_{ch}^2\right)\right)}{\left(1 + cV_{ch}^2\right)^{\frac{3}{2}}}\right)$$
$$\left(\frac{m}{m + V_{ch}^2}\right)dV_{ch} + \int_0^{V_{ds}} qn_{pud}h\left(\frac{m}{m + \left(\dfrac{V_{cs} + V_{cd}}{2}\right)^2}\right)dV,$$

(3.61)

The first term of Eq. (3.61) represents the contribution of Q_t to the drain current and the second term represents the contribution of qn_{pud} to the drain current. The explicit expression (see Eq. (B.1) in Appendix B) of Eq. (3.61) is achieved with the symbolic calculator in Wolfram Mathematica [46].

Similarly, by substituting Eq. (3.45), (3.48), and (3.60) into (3.8), the denominator

integral of Eq. (3.8) can be rewritten as

$$\int_{V_{cs}}^{V_{cd}} \frac{1}{v_F} \left(\frac{1 + fV_{ch}^2}{e + (1 + fV_{ch}^2)g} \right) \left(\frac{m}{m + V_{ch}^2} \right) \left(h + \frac{14z(a + bV_{ch}^2)}{a + bV_{ch}^2 + n_{pud}} \frac{V_{ch}}{\sqrt{1 + cV_{ch}^2}} + \right.$$
$$\left. \frac{hd\alpha_{min} \left(2 + cV_{ch}^2 \left(3 + 2cV_{ch}^2 \right) \right)}{\left(1 + cV_{ch}^2 \right)^{\frac{3}{2}}} + \frac{d\alpha_{min} \left(2 + cV_{ch}^2 \left(3 + 2cV_{ch}^2 \right) \right)}{\left(1 + cV_{ch}^2 \right)^2} \frac{14zV_{ch}(a + bV_{ch}^2)}{a + bV_{ch}^2 + n_{pud}} \right) dV_{ch}.$$

$$(3.62)$$

The explicit expression (see Eq. (B.2) in Appendix B) of Eq. (3.62) is calculated with the same symbolic calculator used above.

3.3   Process of Simulation

Fig. 3.14 shows the flow chart of simulation process in Keysight ADS [23]. The simulator sets initial values (usually 0) for all voltages to start up the calculation. The corresponding V_{cd}, V_{cs}, $I_{ds,k}$ are then solved and the current $I_{ds,k}$ is compared with the previously calculated $I_{ds,k-1}$. If the predefined threshold value is not reached, the simulator will update the initial values according to the current $I_{ds,k}$ until the difference between $I_{ds,k}$ and $I_{ds,k-1}$ is smaller than the the predefined threshold. The external and intrinsic voltages are related to each other as

$$V_{d,ext} = V_d + I_{ds,k}R_d \tag{3.63}$$

$$V_{s,ext} = V_s + I_{ds,k}R_s \tag{3.64}$$

where R_d and R_s are the drain and source resistances consisting of both contact and access resistances. $V_{g,ext} = V_g$ as the gate leakage current is negligible and not included in the DC model.
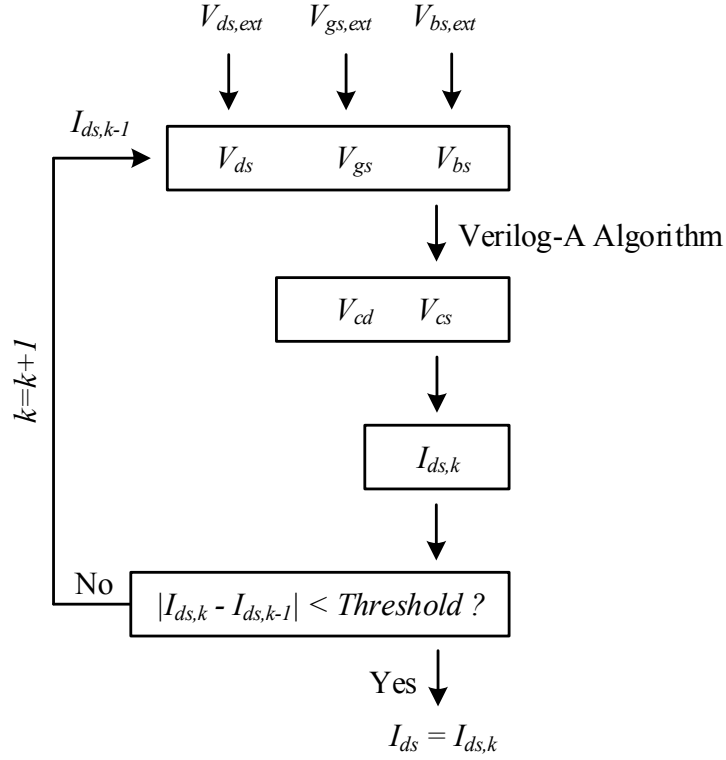
Figure 3.14: Simulation steps and the iteration loop in Keysight ADS.

3.4 GFET Model Validation

The proposed analytical model has been implemented in Verilog-A language and imported in Keysight ADS. In order to verify the GFET drain current model presented in this thesis, the model is first validated against the exact numerical solution results and the simulated transconductance (g_m) is also compared with the model utilizing two-region saturation velocity [25]. Then, the accuracy of the proposed model near the Dirac point is validated by comparing the modelled results with measurement data from a 2.8-μm GFET [32]. Finally, the sound behaviour of the model is compared with a 20 μm $\times$ 15 μm (L $\times$ W) GFET measured inhouse as well as two other GFETs from [47] and [48] under conventional biasing regions.

3.4.1 Numerical vs. Analytical Results

To validate the derivation of the analytical GFET model, the drain current given in Eq. (3.8) is also calculated numerically with Matlab utilising the exact model of α (Eq. (3.52)), C_q (Eq. (3.28)) and μ'_{eff} in both electrostatics and electronic transport calculations. Since the elementary mathematical approximation of first order Fermi-Dirac integral has a maximum relative error as small as 1.79×10^{-6}, it is used in the numerical calculations as well. In Fig. 3.15(a), the numerically calculated charge density at the drain side of a 5-μm GFET against V_{gs} under various V_{ds} is compared with the results achieved from the analytical model. The curves well overlap with each other and the maximum relative error is only 6.77×10^{-4}. In addition, the comparisons of output and transfer characteristics illustrated in Fig. 3.15(b) and (c) also show excellent agreement between the numerical and analytical results. The maximum relative error in the calculated I_{ds} of this GFET is only 2.89 %. Thus, the proposed analytical model, with distinct carrier density dependent mobility for electrons and holes, is in good agreement with the numerically calculated results, regardless of the necessary approximations used to achieve closed-form solutions.

3.4.2 Model vs. Measurements

In the last section, the model has been compared with the numerical results. In order to explore the validation of the analytical model, it is important to compare the simulation results with measurement data. The first step is to extract the fitting parameters (i.e. V_{gs0} V_{bs0}, Δ, μ_n, μ_p, R_d, R_s and m) from the measurement data. The actual physical parameters of the GFET such as thickness of gate dielectric and dielectric constant are also used.

In the first case, the measurement results of L=20 μm and W=15 μm back-gated GFET is used. The device, with 80 nm thick Au contacts, was made of CVD graphene on highly doped Si/SiO$_2$ wafer. The thickness of back gate oxide is 500 nm. In order to
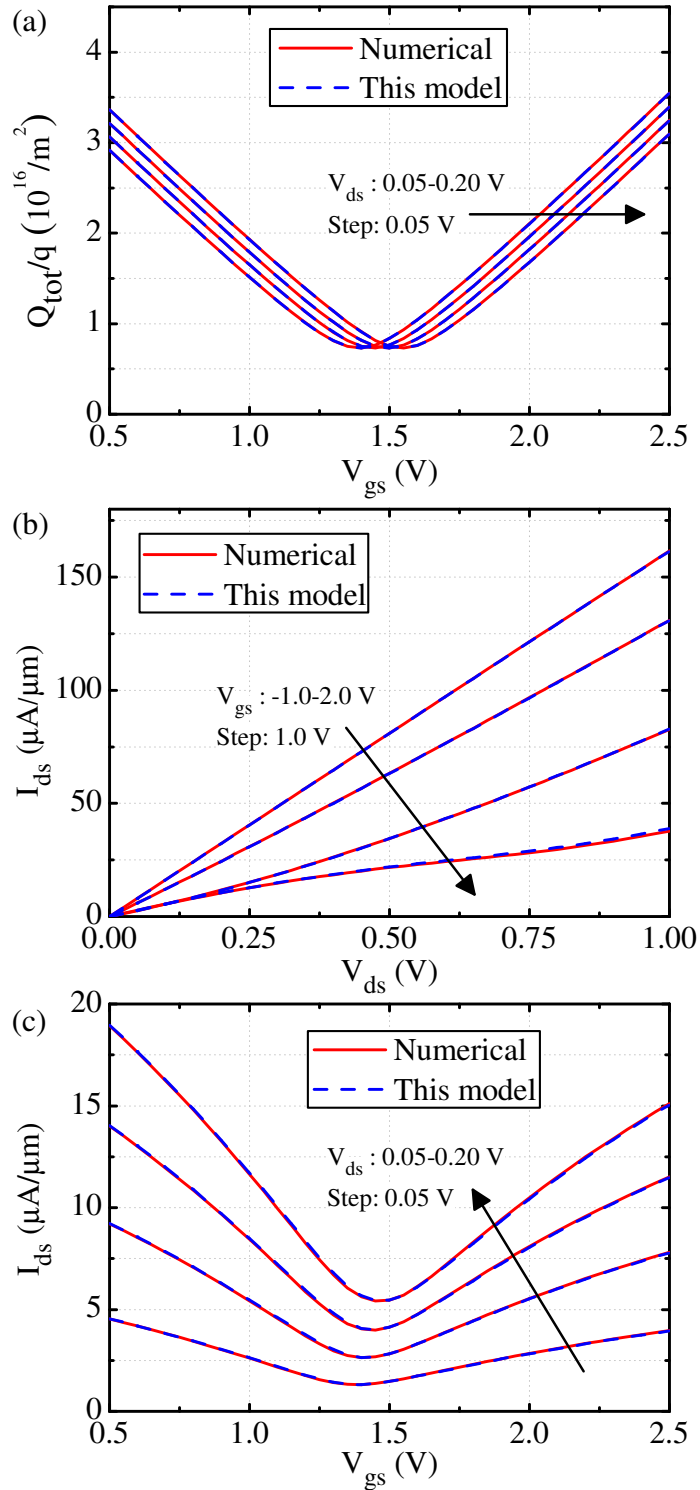
Figure 3.15: (a) The charge density on the drain side (Q_{tot}/q vs. V_{gs}), (b) Output and (c) transfer characteristics of a 5-μm GFET. The results calculated from the analytical model proposed in this thesis is compared with the results achieved from the numerical calculation. Parameters used in the model: $L = 5\,\mu$m, $t_{oxt} = 15$ nm, $k_t = 8.9$, $t_{oxb} = 300$ nm, $k_b = 3.9$, $T = 300$ K, $V_{gs0} = 1.1$ V, $V_{bs0} = 11$ V, $\mu_n = 920$ cm^2/Vs, $\mu_p = 1330$ cm^2/Vs, $\Delta = 92$ meV, $R_{d/s} = 0\,\Omega \cdot \mu$m, $m = 0.1\,V^2$.

remove the effects of water absorbed on the surface of graphene, the GFET was annealed for 12 hours at 380 K in low vacuum, and the measurement was carried out when the device was cooled to room temperature. As shown in Fig. 3.16(a), (b) and (c), the modelled results match very well with the measurement. The low-field electron and hole mobility are 690 and 940 cm^2/Vs, respectively. In the second case, a GFET measured by [47] is used for comparison. It has been shown in [25] that the analytical model with constant carrier mobility cannot accurately describe the transfer characteristic of this device. Therefore, it is important to utilise analytical model with distinct carrier mobility. As shown in Fig. 3.17, both the output and transfer characteristics are well reproduced, demonstrating the novelty of our analytical model. In addition to that, our model can also simulate the saturation behaviour of GFET. In Fig. 3.18 it can be seen that output characteristic of a device with saturation current measured by [48] is reproduced. The fitting parameters used in Fig. 3.17 and 3.18 are on the same level as those used in [25] [47] [48].

3.5 Comparison of GFET Models

As introduced in Section 3.2.2.4, the two-region model of V_{sat} does give a good description of saturation velocity at $q \times |V_{ch}| \ll kT$. However, it results in discontinuous transconductance in the simulation especially when the carrier mobility is high, thus is ill suited to model GFETs. To magnify the discontinuity in g_m for observation, a high carrier mobility of 115,000 cm^2/Vs identical for hole and electron is used instead of 1150 cm^2/Vs. Fig. 3.19 shows the comparison between the simulated g_m from the model introduced in [25] and the model developed in this thesis for the 5-μm GFET measured by [47]. It can be seen that discrepancies appear near the maximum and minimum points of g_m and have been corrected by the proposed model thanks to the improved V_{sat} function (see Eq (3.48)).

In Fig. 3.20, the simulation results of models using different α functions are also
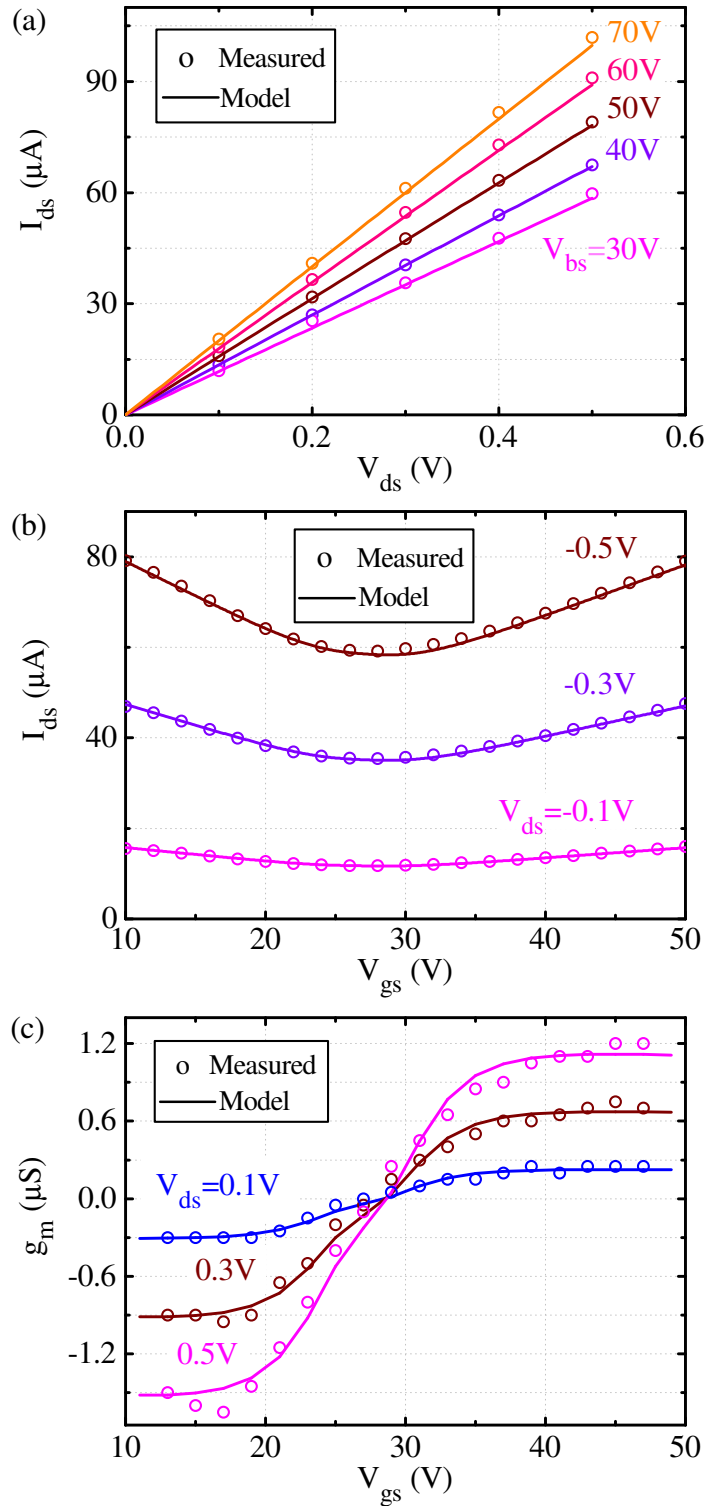
Figure 3.16: Modelled output and transfer characteristics of a $20\,\mu\text{m} \times 15\,\mu\text{m}$ GFET vs. measurement. (a) drain-to-source current I_{ds} against drain-to-source voltage V_{ds} for various back-gate voltage V_{gs} and (b) drain-to-source current I_{ds} against back-gate voltage V_{gs} for various drain-to-source voltages V_{ds} (c) transconductance g_m against back-gate voltage V_{gs} for various drain-to-source voltages V_{ds}. Parameters used in the model: $L = 20\,\mu\text{m}$, $W = 15\,\mu\text{m}$, $t_{oxb} = 500\,\text{nm}$, $k_b = 3$, $T = 300\,\text{K}$, $V_{bs0} = 27.1\,\text{V}$, $\mu_n = 690\,\text{cm}^2/\text{Vs}$, $\mu_p = 940\,\text{cm}^2/\text{Vs}$, $\Delta = 123\,\text{meV}$, $R_{d/s} = 3.75\,\text{k}\Omega \cdot \mu\text{m}$, $m = 1\,V^2$.
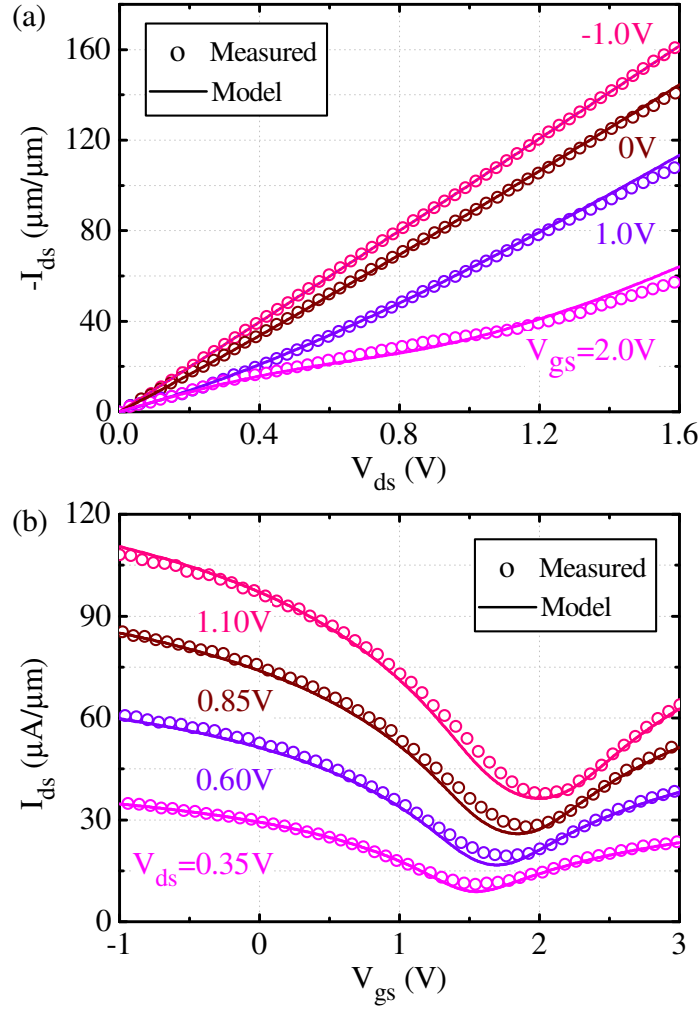
Figure 3.17: Modelled transfer characteristics of a $5\,\mu$m GFET vs. measurement data from [47]. Drain-to-source current I_{ds} against top-gate voltages V_{gs} for various drain-to-source voltage V_{ds}. Parameters used in the model: $L = 5\,\mu$m, $t_{oxt} = 15\,$nm, $k_t = 8.9$, $t_{oxb} = 300\,$nm, $k_b = 3.9$, $T = 300\,$K, $V_{gs0} = 1.1\,$V, $V_{bs0} = 11\,$V, $\mu_n = 920\,$cm^2/Vs, $\mu_p = 1330\,$cm^2/Vs, $\Delta = 92\,$meV, $R_{d/s} = 2\,$k$\Omega \cdot \mu$m, $m = 0.1\,V^2$.

compared with each other. One can see the simulation results from the model proposed in this work agree well with the measured data from [32]. The model using $\alpha = 0.5$ differs from the measurement near the Dirac point and overlaps with the proposed model at high V_{ch}. The overestimation caused by using $\alpha = 1$ at $q \times |V_{ch}| \gg kT$ is shown by the red dash-dotted line.
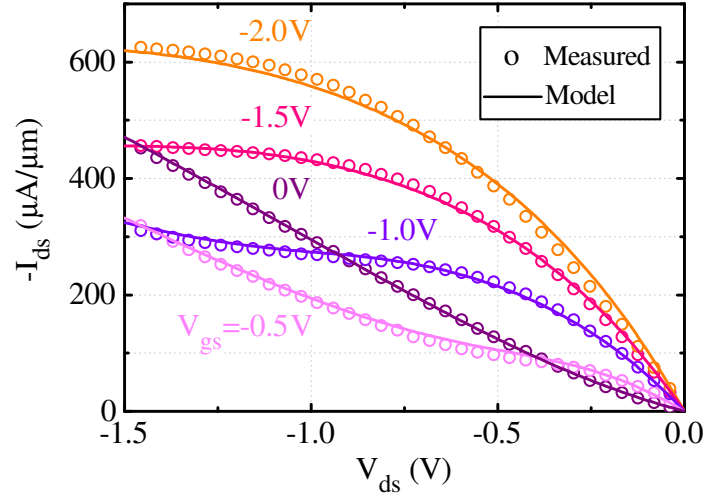
Figure 3.18: Modelled output characteristics of a $3\,\mu$m GFET against measurement data from [48]. Drain-to-source current I_{ds} against drain-to-source voltage V_{ds} for various gate-to-source voltages V_{gs}. Parameters used in the model: $L = 3\,\mu$m, $t_{oxb} = 8.5$ nm, $k_b = 3.5$, $T = 300$ K, $V_{bs0} = -0.07$ V, $\mu_n = 6500\,\text{cm}^2/\text{Vs}$, $\mu_p = 7700\,\text{cm}^2/\text{Vs}$, $\Delta = 66$ meV, $R_{d/s} = 120\,\Omega \cdot \mu$m, $m = 0.5\,V^2$.
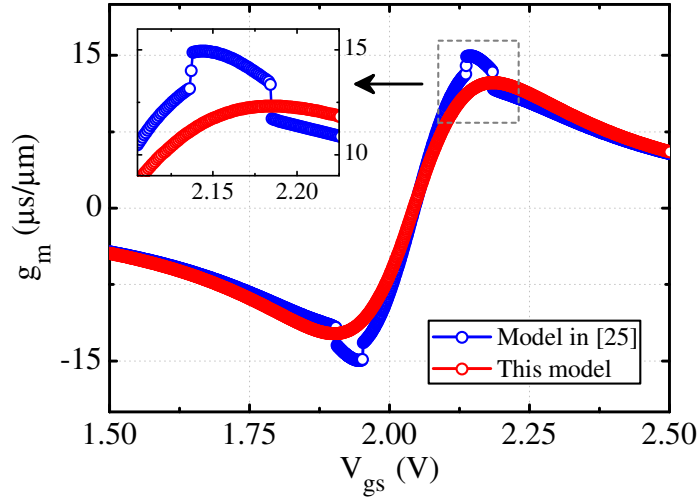
Figure 3.19: Comparison of the modelled transconductance g_m vs. top-gate voltage V_{gs} (V_{ds}=1.1 V) of a $5\,\mu$m GFET [47] in this work and a model with two-region saturation velocity [25]. Parameters used in the model are taken from [25] except the carrier mobility: $L = 5\,\mu$m, $t_{oxt} = 15$ nm, $k_t = 8.9$, $t_{oxb} = 300$ nm, $k_b = 3.9$, $T = 300$ K, $V_{gs0} = 1.24$ V, $V_{bs0} = 11$ V, $\Delta = 100$ meV, $R_{d/s} = 3.5\,\text{k}\Omega \cdot \mu$m (and $m = 10\,V^2$ for this work, $\hbar\Omega = 75$mV for [25]). $\mu_n = \mu_p = 115,000\,\text{cm}^2/\text{Vs}$ is used here instead of the original $1150\,\text{cm}^2/\text{Vs}$ to magnify the discontinuity of g_m.
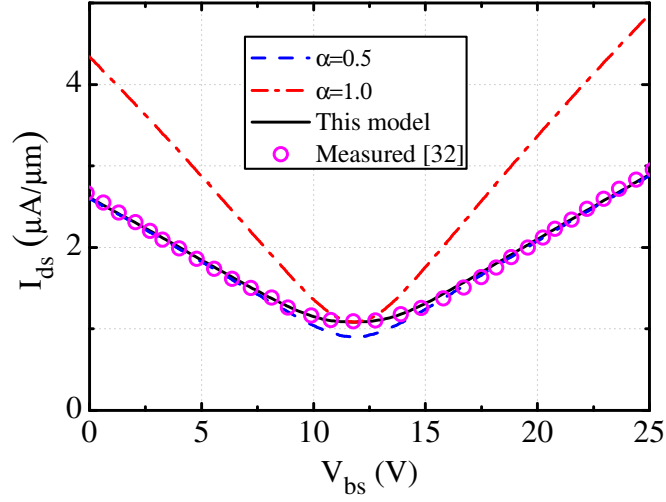
Figure 3.20: Comparison of the modelled drain to source current I_{ds} vs. back-gate to source voltage V_{bs} of a $2.8\,\mu$m GFET [32] in this work and models using constant α. Parameters used in the models: $L = 2.8\,\mu$m, $t_{oxb} = 285\,$nm, $k_b = 3.9$, $T = 300\,$K, $V_{bs0} = 11.86\,$V, $\mu_n = 430\,$cm^2/Vs, $\mu_p = 410\,$cm^2/Vs, $\Delta = 64\,$meV, $R_{d/s} = 100\,\Omega \cdot \mu$m, $m = 0.5\,V^2$.

Table 3-A: Details of GFET model comparison

GFET Model	Closed-form	C_q approximation	Distinct Q_{net} & Q_{tot}	V_{sat} model	μ model	Distinct μ_p & μ_n
[14]	yes	$\propto |V_{ch}|$	NA	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[15]	no	$\propto |V_{ch}|$	no	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[16]	no	$\propto |V_{ch}|$	yes	2 regions	constant	no
[17]	yes	$\propto |V_{ch}|$	no	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[18]	yes	$\propto \sqrt{1 + c_c^2 V_c^2}$	yes	NA	constant	no
[19]	yes	$\propto |V_{ch}|$	no	constant	constant	no
[20]	yes	NA	NA	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[21]	yes	$\propto |V_{ch}|$	no	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[22]	yes	NA	NA	constant	constant	no
[24]	yes	$\propto |V_{ch}|$	yes	$\propto \left|V_{ch}^{-1}\right|$	constant	no
[25]	yes	$\propto \sqrt{1 + c_c^2 V_c^2}$	yes	2 regions	constant	no
[32]	yes	$\propto |V_{ch}| + $ constant	NA	$\propto \left|V_{ch}^{-1}\right|$	constant	yes
[34]	yes	$\propto |V_{ch}|$	NA	$\propto \left|V_{ch}^{-1}\right|$	constant	yes
[35]	yes	NA	NA	$\propto \left|V_{ch}^{-1}\right|$	constant	yes
[36]	yes	$\propto |V_{ch}| + $ constant	no	$\propto \left|V_{ch}^{-1}\right|$	constant	yes
[37]	yes	NA	NA	$\propto \left|V_{ch}^{-1}\right|$	empirical	no
[26]	yes	NA	NA	$\propto \left|V_{ch}^{-1}\right|$	empirical	no
This work	yes	$\propto \sqrt{1 + c_c^2 V_c^2}$	yes	approx. of 2 regions	empirical	yes

At last, in order to make a more complete comparison with other work, several GFET models with different modelling techniques and parameters are summarised in Table 3-A.

3.6   Conclusion

In this chapter, the multiscale modelling approaches of graphene transistors have been introduced. The first-principle and atomistic modelling methods are suitable for predicting the performance of atomic scale devices. The semiclassical device modelling approach can be used to simulate relatively larger devices with physical insight. Due to the requirement of circuit analysis, the analytical models with closed-form expressions are derived from the semiclassical models using empirical models and fitting parameters. In Section 3.2, the derivation of a novel Verilog-A compatible analytical model of GFET for circuit analysis has been presented. The variation of mobility against carrier density is included as well as the distinct electron and hole mobility. The proposed model is capable of simulating both electron and hole conduction of GFET simultaneously. It can be implemented in Keysight ADS for circuit analysis. The model has been validated against measurement results and the comparison between proposed model and other existing GFET models is also illustrated, demonstrating the novelty of this research work.

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Chapter 4

Graphene Non-Foster Circuits

In this chapter, the developed drift-diffusion model is used to explore the implementation of GFET in non-Foster circuit. Before going to the details of NFC design, an overview on the performance of GFET in other RF circuits such as mixers and amplifiers will be presented. This is followed by an introduction of NFC background and theories. Then, two different approaches to realise negative impedance namely Linvill's technique and NDR-based NFC are conducted. The stability analysis associated with negative impedance is also discussed.

4.1   Graphene RF Circuits Review

As introduced in Chapter 1, there are different approaches to realise graphene-based transistors. Compared with the conventional top-gated GFET, bilayer GFET provides better drain current saturation for analog/RF circuits due to the existence of the field-induced bandgap. However, the corresponding parasitics are also increased due to the additional back gate used for bandgap opening. The lateral graphene tunnelling and GNR FETs are more likely to find applications in logic circuits because of their high on-off ratios. The vertical graphene tunnelling transistors demonstrate both high on-off

ratio and negative differential resistance that can potentially be used in both digital and analog/RF applications. The HETs with graphene base have demonstrated high on-off ratio and drain current saturation but their transfer ratio still needs to be improved hopefully through the device geometry optimization. So far, most of efforts have been devoted to the implementation of conventional single-gated GFETs. The high carrier mobility of graphene makes it super promising for high frequency electronics. The ambipolar conduction of graphene can potentially simplify the circuits of phase shift keying, RF mixer, etc.

4.1.1 Frequency Doubler and Mixer

In 2009, the first graphene frequency doubler based on the ambipolar characteristic of GFET was demonstrated by Wang et al. [1]. The circuit consists of a single back-gated GFET and a known resistor R_0. The GFET is biased in CS mode with input signals fed to the gate. The output signal is read out at the drain, exhibiting excellent spectral purity due to the sublinear transfer characteristic of GFET. The device showed a voltage gain of 1/200 and it was for the first time that frequency doubling was achieved with a single transistor design, yielding simplified schematic for frequency doubling circuits. Although the author only demonstrated a measured frequency-doubling effect up to 10 kHz because of the limitation in their measurement setup, the circuit can potentially operate at higher frequencies. The next year, another frequency doubler utilising the top-gated GFET was reported by another research group [2]. Frequency doubling with a maximum input frequency of 200 kHz was demonstrated experimentally. Due to the improved transconductance of the top-gate configuration, the voltage gain of this device is ten times that of the first doubler.

In 2010, Wang's group presented a RF mixer utilising the ambipolar transport property of GFET [3], operating around a maximum frequency of 10 MHz with conversion loss between 30 to 40 dB. As shown in Fig. 4.1(a), both RF and local oscillator (LO) signals are fed from the gate and the intermediate frequency (IF) signal is read out at
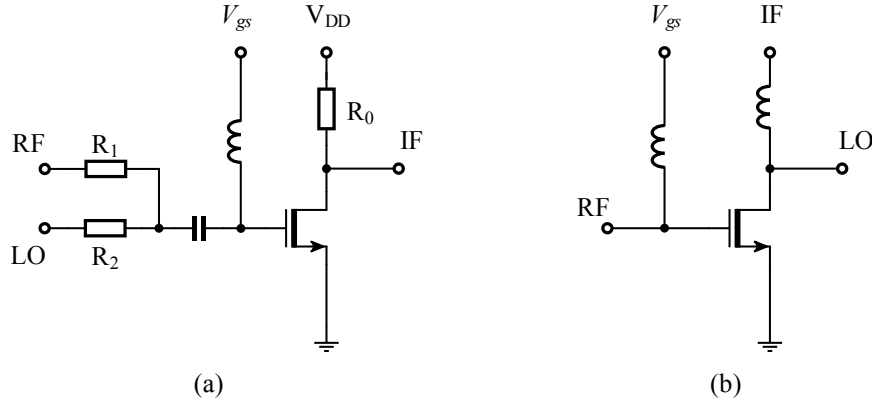
Figure 4.1: GFET RF mixers based on (a) ambipolar transfer characteristic (b) gate-induced electrostatic modulation.

the drain. Thanks to the the symmetrical transfer characteristic of GFET, a measured input third-order intercept point (IIP3) as high as 13.8 dBm was achieved. In 2011, a similar RF mixing or doubling circuit operating at 1 to 10 GHz was presented utilising a GFET fabricated on glass substrate with self-aligned nanowire gate [4]. Although the measured conversion loss is as large as 55 dB at 4 GHz due to the impedance mismatch and non-optimized measurement setup, it was for the first time that frequency mixing or doubling was achieve with GFETs in gigahertz regime. The IIP3 as high as 13.5 dBm was achieved with this device, comparable to that of Wang's mixer. Also in 2011, a monolithic GFET mixer fabricated on silicon carbide substrate was also reported [5]. As the first fully-integrated GFET circuit, this mixer exhibits a broadband operation at a maximum frequency of 10 GHz. Different from the mixers based on the ambipolar transfer characteristic, this device utilised the gate-induced electrostatic modulation of GFET channel resistance. As shown in Fig. 4.1(b), the LO and RF signals in this device are applied to the drain and gate respectively, resulting in a nonlinear relation between the drain current and the gate & drain voltages: $I_{ds} \approx A \cdot (B + g_m \cdot V_{gs}) \cdot V_{ds}$. Here coefficients A and B are constants to be decided and the power of IF signal is proportional to the product of g_m and g_{ds}. Hence, high-k dielectric material HfO_2 was used in the top-gated GFET, resulting in about 10 times transconductance enhancement. The mixer utilising this high-transconductance GFET demonstrated an improved conversion loss of 27 dB at 4 GHz. This work paves the way for other GFET-based fully-integrated

RF circuits.

The mixers introduced so far all utilise fundamental frequency components to generate the IF signal. In 2012, a subharmonic GFET mixer utilising only half the LO frequency used in fundamental mixers was proposed [6]. As shown in Fig. 4.2(a), the GFET in this mixer was also biased in common-source mode but the RF signal was fed from the drain. IF signal is also read out at the drain with bandpass filters isolating the RF and IF ports. LO signal is applied to the gate. A bias-T was used at the gate for impedance matching of the LO port. Assume the GFET has symmetry transfer characteristic and is properly biased at the Dirac point, the gate modulation due to LO signal varies the channel resistance R_{ds} at a frequency of $2f_{LO}$. Thus, the resulting frequency of IF signal is $f_{IF} = |f_{RF} - 2f_{LO}|$. The subharmonic mixer allows the use of lower LO frequency compared to the fundamental mixer. This is very promising for applications at millimetre wavelengths where a powerful LO source is hard to achieve. In addition, due to the large frequency difference between RF and LO signals, better RF-to-LO port isolation is obtained compared with the fundamental mixers. The proposed subharmonic is design for a 50 Ω system, exhibiting 24 dB down-conversion loss at $f_{RF} = 2$ GHz, $f_{LO} = 1.01$ GHz and $f_{IF} = 20$ MHz. In 2015 and 2017, the GFET-based subharmonic mixers operating around 30 GHz and 200 GHz were also demonstrated experimentally by the same research group [7, 8]. The graphene channel consisting of patterned bow-tie structures was used in these devices to achieve a 50 Ω port impedance and higher on-off ratio. Another advantage of using patterned graphene channel is the reduced gate capacitance as part of the channel material has been etched away. This reduced gate capacitance helps to increase the GFET performance at higher frequencies. These mixers exhibited the conversion loss of 18 dB at 27 GHz and 29±2 dB around 200 GHz.

In 2013, a passive GFET-based mixer was presented by Moon et al. [9]. As shown in Fig. 4.2(b), the schematic and feeding procedure of this zero-bias mixer is similar to that of the subharmonic mixer but without DC bias at the drain. Thus, it does not consume DC power. The device has been experimentally demonstrated at a maximum
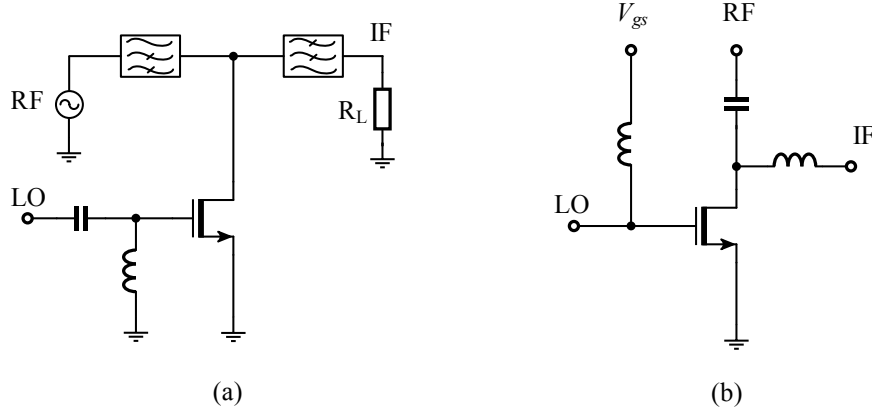
Figure 4.2: GFET RF mixers (a) subharmonic (b) zero-bias.

frequency of 20 GHz with 18 dB conversion loss. The minimum conversion loss of 14 dB was achieved at 2 GHz and an IIP3 as high as 27 dBm was also measured under a small LO power of 2.6 dBm. As the linearity of mixer is usually worse than that of other blocks in a RF receiver, the upper limit of intermodulation performance for the overall system is often determined by the mixer [10]. Therefore, this high linearity passive mixer is highly preferred in low-noise high-linearity RF systems.

In 2015, the first double-balanced GFET mixer with differential ports was experimentally demonstrated [11]. The device consists of four GFETs, fabricated on Si/SiO_2 substrate in cross-coupled configuration, and other passive on-chip components including four inductors and four capacitors. The off-chip baluns are implemented to convert the differential ports of the GFET IC into single-end mode. The passive mixer in this design requires no DC bias, making the device tolerant for variations in the fabrication process. High linearity is also guaranteed by the double-balanced structure through suppressing the even-order non-linearities. A high IIP3 of 21 dBm has been measured with a LO power of -2.6 dBm at 3.5 GHz regardless of the GFET mismatch. Another advantage of double-balanced mixer is the excellent RF-to-IF and LO-to-IF isolations of up to 21 and 38 dB, respectively. Although the mixer demonstrates high conversion loss around 30 dB, it is possible to implement a low-noise amplifier in series utilising the saved DC power.

4.1.2 Amplifier

GFET is different from the silicon or III-V transistor primarily due to its ambipolar transfer characteristic. Utilizing this unique property, the first triple-mode amplifier based on a single GFET was presented in 2010 [12]. The device is able to switch among CS, CD and frequency multiplication modes through the tuning of bias voltage. Both phase shift keying (PSK) and frequency shift key (FSK) were demonstrated with this single transistor device, greatly simplifying their circuit realisations. However, the gain of this amplifier is only between $0.01{\sim}0.02$ due to the low g_m and poor drain current saturation of GFET (please note the gain in this section is voltage gain under open-circuit or large-load-resistance condition unless otherwise stated). Meanwhile, the gain mismatch observed during the PSK and FSK modulation can significantly increase the bit-error rate. The authors attribute this mismatch to the asymmetry transfer characteristic of the GFET and the performance difference between CS and CD modes. They suggest that the former effect can be minimized by optimizing the fabrication process to reduce the doping of graphene channel and the later issue can be removed by the use of a feedback loop and differential outputs.

In 2011, the first GFET amplifier demonstrating AC voltage gain was reported [13]. As illustrated in [14], the drain current saturation of GFET can be improved by decreasing the equivalent oxide thickness (EOT) of the gate dielectric. Therefore, in this work the authors used 4-nm thick HfO_2 as the gate dielectric, resulting in an ultrathin EOT of 1.75 nm and an extrinsic transconductance as high as 1.2 mS/μm. The GFET, with 500-nm channel length, is folded in multi-finger configuration to reduce the gate resistance. The CS amplifier exhibits a maximum voltage gain around 5 dB at low frequencies and a -3 dB bandwidth exceeding 6 GHz. Later in that year, Guerriero et al. utilised the complementary configuration of a GFET pair to achieve 11.4 dB gain at 10 kHz [15]. This audio amplifier shows a -3 dB cutoff frequency up to 70 kHz and a unity-gain frequency of 360 kHz. In 2012, Wu et al. reported their GFETs with both voltage and power gain approaching 20 dB [16]. Their experimental results show a clear voltage

gain improvement from -7 to 8 dB while the EOT scales from 20 to 3 nm. They also demonstrated the first wafer-scale integrated GFET amplifier exhibiting more than 3 dB voltage gain at 5MHz.

In 2015, a GFET-based four-stage distributed amplifier were fabricated on printed circuit board (PCB) [17]. Although their simulation results seems promising, the measurement results depicts a voltage gain of -20 dB and a bandwidth of 1.5 GHz with 50 Ω load. In 2016, the first GFET-based low-noise amplifier MMIC with impedance matching networks at both input and output were presented [18]. The measurement shows a AC power gain of 3.4 dB at 14.3 GHz and a minimum noise figure of 6.2 dB with 50 Ω load resistance. Although the amplifier suffers from poor S_{11}, it is a significant exploration towards microwave frequency application of GFET. Recently, Song et al. reported their GFET amplifiers fabricated on lightly doped silicon substrate [19]. As the silicon substrate induces additional charge to graphene that lowers the graphene/metal contact resistance, these devices demonstrated smaller contact resistance compared with the GFET on insulating substrate. In addition, the measurement results also reveal that the residual carrier concentration on graphene/Si interface is decreased compared with that of the graphene/SiO$_2$ devices. Since the maximum $r_o = 1/g_{ds}$ increases while the residual carrier concentration and R$_C$ decreases, the drain current saturation of graphene-on-silicon FET is improved compared to conventional graphene-on-insulator FET. Moreover, due to the higher phonon energy of silicon, these graphene-on-silicon FETs also exhibit higher carrier mobility. The measured maximum r_o of 2.5 M$\Omega \cdot \mu$m and maximum intrinsic voltage gain of 28 dB are almost comparable to the Si MOSFETs.

4.1.3 Oscillator and RF Receiver

Except mixers and amplifiers, graphene ring oscillator operating at a maximum frequency of 1.28 GHz has also been reported in 2013 [20]. The oscillator consists of four complementary dual-gated GFET inverters, with the last stage acting as a output buffer. In order to explore the effect of channel scaling to the oscillator, three devices utilising

GFETs with different channel lengths were fabricated. By changing the supply voltage, their oscillation frequency can be tuned between 284-350 MHz ($L = 3\,\mu m$), 504-750 MHz ($L = 2\,\mu m$) and 1-1.28 GHz ($L = 1\,\mu m$), respectively. Unfortunately, due to the unintentional doping of graphene during the fabrication, these oscillators require large back-gate voltage up to 200 V to move the Dirac-point back to zero V_{gs} for inverter operation. What is worse, the large hysteresis introduced by the back gate can further drive the restored Dirac-point towards higher V_{gs} and damage the circuit oscillation. In spite of these drawbacks, this circuit can also provide mixing function, with the first three stages acting as a built-in LO source and the last stage as the main mixer. The device suffers from poor RF feedthrough as no isolation circuits is applied between RF and IF ports. A conversion loss of 19.6 dB was measured with -18.5 dBm LO power.

Later in that year, another graphene ring oscillator utilising local back-gated GFETs was presented [21]. The reduced graphene doping and improved transconductance enable the realisation of high-performance stable ring oscillators. The devices composed of five inverting stages demonstrates a fundamental oscillation frequency up to 40 MHz. This relatively low oscillation frequency is caused by the lower carrier mobility and large parasitic capacitances induced by the overlapping between local back gate and the source & drain electrodes.

In 2014, an important milestone happened in the development of graphene-based integrated circuits. IBM researchers fabricated the first GFET integrated RF receiver on 200 mm silicon substrate [22]. The circuit is composed of a two-stage bandpass amplifier and a RF mixer, consuming a chip area of 0.6 mm^2 only. The buried T-shaped multi-finger gate structure is used to improve the f_{max} of GFETs. The CMOS-compatible passive-first active-last fabrication process preserves the high quality of CVD-grown graphene. It is noted that the silicon substrate remains unused in this design. Thus, the GFET RF circuits can be fabricated on the top of silicon-based logic circuits to realise compact ultra-low cost chips for modern communication systems. The measured conversion loss of this RF receiver is 10 dB with -2 dBm LO power at f_{RF}=4.3 GHz.

Consequently, the IC can also operate as a pure amplifier if a supply voltage is applied to the drain of GFET in the mixer stage instead of the IF signal. It was for the first time that a positive power gain of 4 dB was achieved with GFET amplifier in 50 Ω system.

4.1.4 Conclusion

Although the experimental results of the GFET RF circuits are still not as good as the devices utilising Si MOSFETs or III-V transistors due to the immature fabrication techniques and improper material selection, GFETs have shown their potential in the development of RF devices such as high-linearity passive mixers. With the improvement of fabrication technology, the RF performance of GFET can also be improved and the ultrahigh carrier mobility of graphene may provide great advantage at high frequency applications. In the rest of this chapter, we aim to explore the implementation of GFET through non-Foster circuits. With the GFET model developed in Chapter 3, the NFCs utilising two different techniques are simulated.

4.2 Overview of Non-Foster Circuit

The size reduction of antenna at low frequencies such as VHF band requires the implementation of electrically small antennas (ESAs). Broadband impedance matching of ESA is a challenge for antenna engineers due to the Bode-Fano limitations [23, 24]. The traditional passive matching method utilising capacitive and/or inductive components leads to high quality factor and narrow bandwidth. To improve the bandwidth of ESAs, active impedance matching as shown in Fig. 4.3 is proposed. Since NFCs exhibit monotonically decreasing reactance with the increase of frequency, they can be used as active matching networks to cancel the reactance of ESAs and obtain infinite bandwidth in theoretical sense, as shown in Fig. 1.4(b). In addition, the application of NFCs has been extended to the bandwidth improvement of metamaterial structures as well [25, 26].

Depends on the antenna input reactance
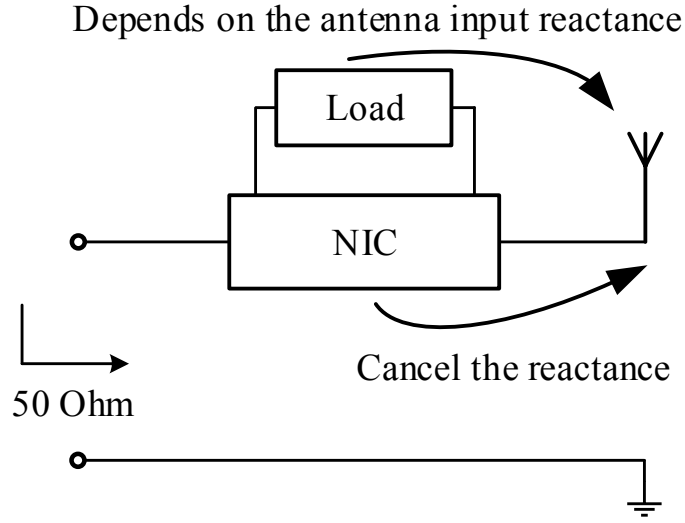
Figure 4.3: Block diagram of non-Foster matching topology.

4.2.1 H-model of Non-Foster Circuit

Generally, the NFC is a two-port network that can be designed as either floating or single-ended, as shown in Fig. 4.4. Ideally, a NFC can be represented as an equivalent *h*-model of a two-port network, as shown Fig. 4.5. It is easy to achieve the relations below:

$$\begin{pmatrix} V_{in} \\ I_{out} \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} I_{in} \\ V_{out} \end{pmatrix} \tag{4.1}$$

Eq. (4.1) can be rewritten as

$$V_{in} = h_{11}I_{in} + h_{12}V_{out}, \tag{4.2}$$

and,

$$I_{out} = h_{21}I_{in} + h_{22}V_{out}, \tag{4.3}$$

Hence, the input impedance is written as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = h_{11} - \frac{kZ_L}{1 + h_{22}Z_L}. \tag{4.4}$$
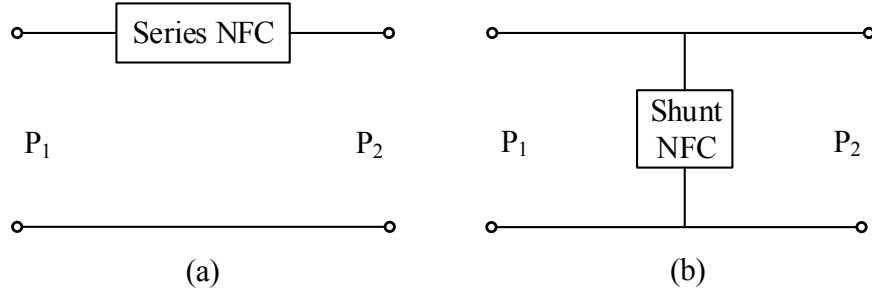
Figure 4.4: Diagram of Floating (a) and single-ended (b) NFC.
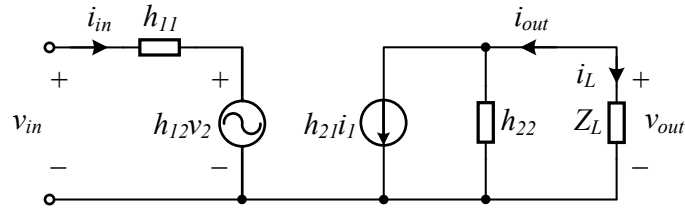
Figure 4.5: The h-model of NFC.

where $k = h_{12}h_{21}$ and $Z_L = -V_{out}/I_{out}$. If $h_{11} = h_{22} = 0$, Eq. (4.4) is simplified to

$$Z_{in} = -kZ_L. \tag{4.5}$$

For an ideal NFC where $h_{11} = h_{22} = 0$ and $k = h_{12}h_{21} = 1$, the input impedance is equal to the reversed load impedance $-Z_L$. It is noted that there are two possibility that can lead to $k = 1$:

$$h = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \text{ or } \begin{pmatrix} 0 & -1 \\ -1 & 0 \end{pmatrix}. \tag{4.6}$$

In the first case, $h_{12} = h_{21} = 1$ results in $V_{in} = V_{out}$ and $I_{in} = I_{out} = -I_L$. Thus, it looks as if the NFC transfers input voltage and current from input to output with voltage phase unchanged but current phase inverted. This kind of circuit is named current-inversion NFC. In the second case, $h_{12} = h_{21} = -1$ leads to $V_{in} = -V_{out}$ and $I_{in} = -I_{out} = I_L$. Hence, the voltage phase is inverted at the output while current phase stays the same. This kind of circuit is named voltage-inversion NFC.

4.3   GFET-based Linvill's Non-Foster Circuit

As introduced before, there are several approaches to achieve negative impedance. Linvill's technique has been widely used with BJTs and CMOS (or BICMOS) process due to its broadband and high frequency operation. In this section, the exploration of utilising GFET for Linvill's NFC design is presented.

4.3.1   Linvill's Non-Foster Circuit Technique

Linvill's NFC belongs to the floating voltage-inversion type. It utilises a pair of BJTs connected as a feedback loop, in which the current is driven from lower to higher potential across the load, as shown in Fig. 4.6. Thus, it appears as a negative component at the input port. If the input port is defined as the emitters of the BJTs, the circuit is open circuit stable (OCS), indicating the NFC is stable when the input port is open circuited in an extreme case [27]. On the other hand, if the input port is defined as the collectors of the BJTs, the circuit is short circuit stable (SCS), indicating the NFC is stable when the input port is short circuited in an extreme case [27]. In this thesis, we explore the feasibility of utilising GFETs for Linvill's OCS NFC.

4.3.2   GFET Selection

As depicted in Chapter 2, GFET exhibits poor drain current saturation that limits its application in analog/RF circuits. Although the saturation behaviour of GFET can be improved by decreasing the thickness of gate dielectric, it is still hard to achieve power gain from GFET amplifiers for 50-Ω systems. Meanwhile, the large hysteresis observed in poorly fabricated GFET can heavily degrade the performance of the circuits. Hence, in this work we use the GFET whose output characteristic has been well reproduced with our drift-diffusion model (see Fig. 3.18). As this GFET utilises h-BN-encapsulated graphene as channel material, the hysteresis is decreased to less than 1 mV. Although
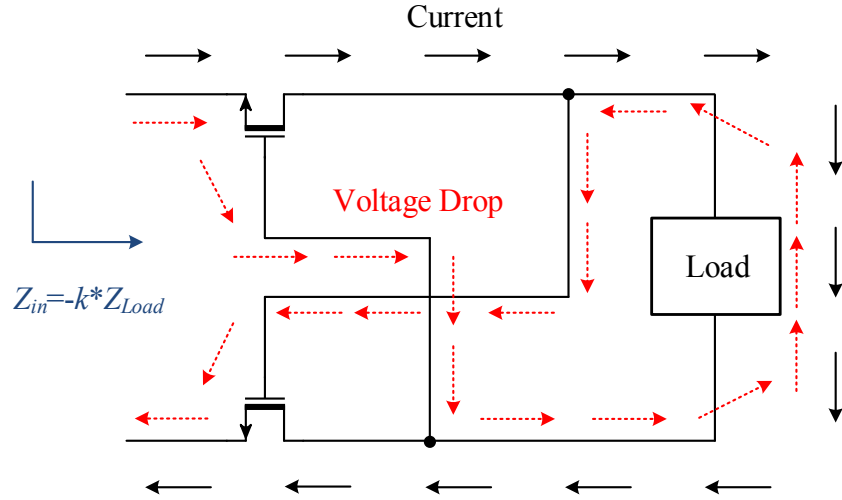
Figure 4.6: Typical voltage current relationship of Linvill's NFC model having current flow from lower to higher potential at the load.

this device may not exhibit the best saturation behaviour, the measured saturation current and its excellent hysteresis performance make it a good candidate for Linvill's NFC design.

The channel width of GFET is chosen through a series of simulations. When the width increases, higher g_m can be achieved but the output resistance r_{ds} would be reduced. This contradiction is not important in BJTs and CMOS transistors due to their high r_{ds}. But GFET's poor saturation current do not allow us to achieve both high g_m and high r_{ds} at the same time. Therefore, a proper width (W) to length (L) ratio should be determined as a compromise. In this work, the channel size of $W = 30\,\mu$m and $L = 3\,\mu$m is chosen for the proposed circuit.

The frequency response of GFET is conducted by including the necessary parasitics. The full parasitic capacitance models of GFET have been derived theoretically by Jimenez in 2011 [29], as depicted in Appendix B. Later in 2012, it was experimentally shown that the large-signal model, as shown in Fig. 4.7, with internal and external parasitics is sufficiently enough to accurately represent the frequency response of a GFET [28]. Hence, in this thesis, the DC model of GFET is combined with parasitics given as Fig. 4.7 to form the large-signal model for NFC analysis. The external parasitics of
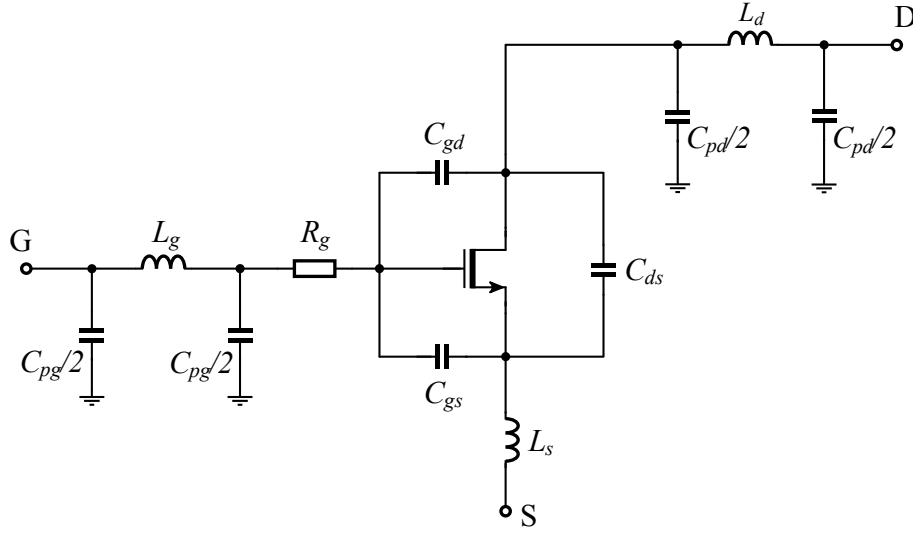
Figure 4.7: Schematic of GFET with parasitics [28]. $C_{gs} = 280\,\text{fF}$, $C_{gd} = 50\,\text{fF}$, $C_{ds} = 150\,\text{fF}$, $C_{pd} = 40\,\text{fF}$, $C_{pg} = 40\,\text{fF}$, $L_s = 75\,\text{pH}$, $L_d = 75\,\text{pH}$, $L_g = 75\,\text{pH}$, $R_g = 12\,\Omega$.

standard contact pads extracted in [28] are used in our simulation.

4.3.3 NFC Design

The classic four-resistor bias circuit, as shown in Fig. 4.8, is used in this design to provide DC bias for GFET. The resistors R_{g1} and R_{g2} should be large enough to reduce the power consumption. The drain and source resistances R_d and R_s are chosen as small as possible to reduce the supply voltage. The Q-point of GFET is chosen at $V_{gs} = -1.5\,\text{V}$ and $V_{ds} = -1.5\,\text{V}$, within the measurement range, to guarantee more realistic analysis for the circuit simulation. The corresponding transconductance and output resistance are $g_m = 8\,\text{ms}$ and $R_{ds} = 3.2\,\text{k}\Omega$, respectively.

The schematic of the simulated NFC is depicted in Fig. 4.9. In order to achieve more realistic results, the electromagnetic (EM) model of a PCB layout,as shown in Fig. 4.10, is also included. It was designed for a BJT based NFC [30] and the validity has been proved through measurement. The footprints of all realistic components excluding GFETs have been taken in account in the EM model.
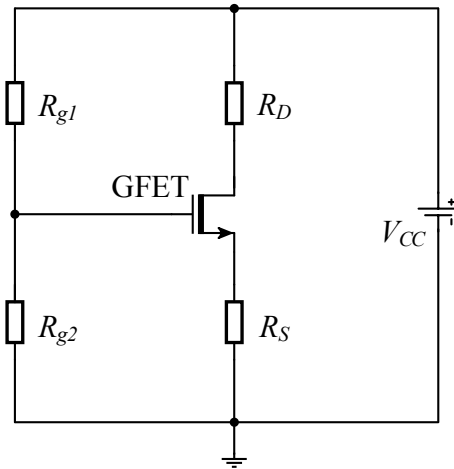
Figure 4.8: Schematic of four resistor bias circuit.
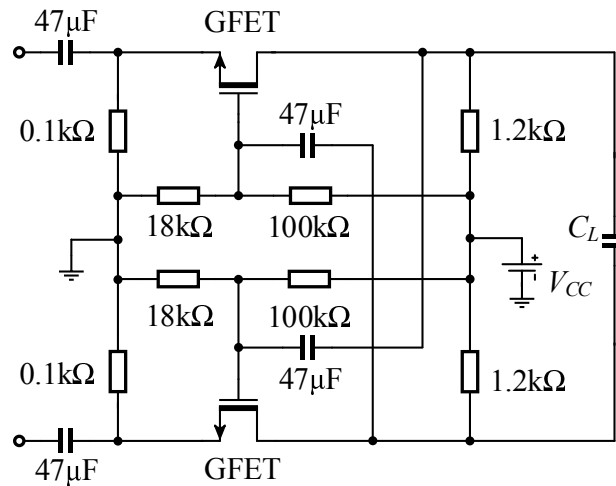
Figure 4.9: Schematic of the NFC simulated in this work.

As shown in Fig. 4.11(a), the simulation results under different load conditions are presented. It can be seen that the resulting negative capacitance is positively proportional to the load capacitance. Similar tuning can also be achieved by varying the supply voltage (see Fig.4.11(b)). Due to the low r_{ds} of GFET, the negative capacitance is not constant against frequency and the maximum frequency of operation is limited to 200 MHz.
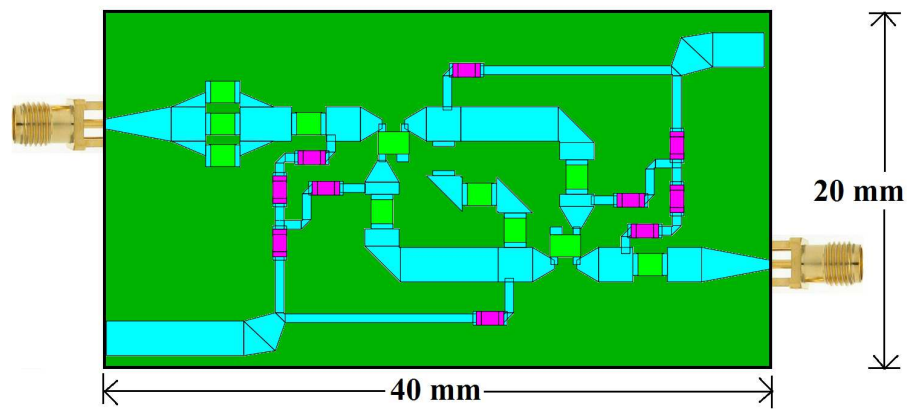
Figure 4.10: Layout including footprint of real components (except the GFET footprint) [30].
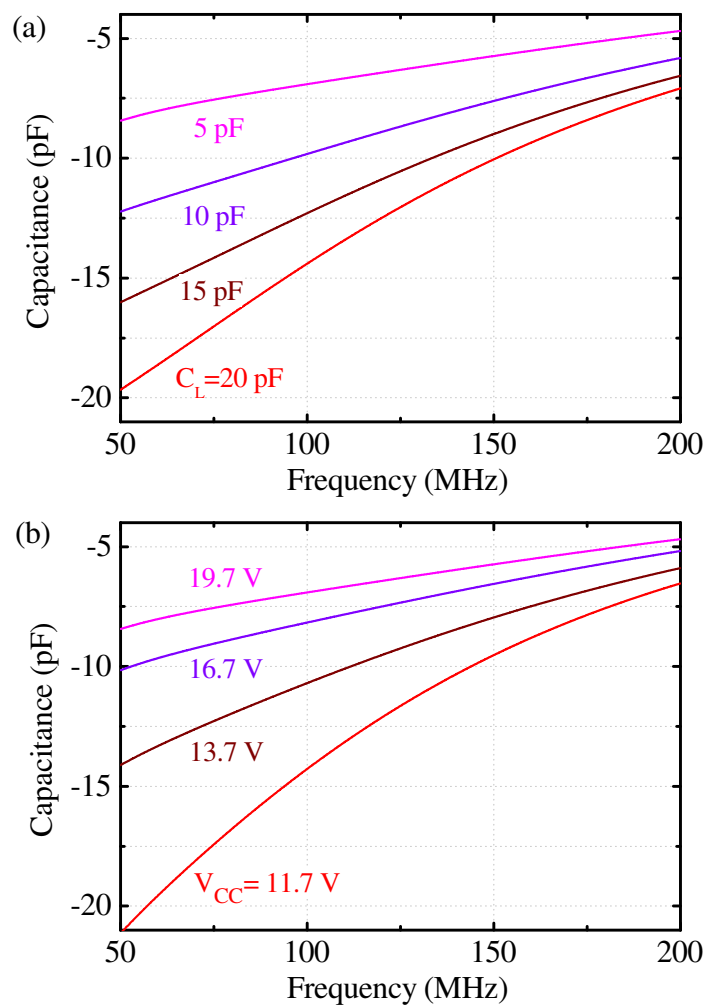
Figure 4.11: Simulated capacitance of the proposed NFC: (a) load tuning (b) voltage tuning.

4.3.4   Stability Analysis

As a negative impedance device, the NFCs are highly likely to oscillate and perform as a oscillator rather than a negative impedance element. Therefore, stability analysis is an important issue during the application of NFCs. It is necessary to stabilise the NFC during their implementations. For instance, when NFCs are used for active impedance matching of ESA, the ESA's input impedance should act as a stability element to prevent the NFC from oscillating.

As we know, there are several approaches for stability analysis of oscillators and amplifiers. The traditional pole-zero analysis is too complicated for high-order complex networks and the Rollet's k factor test have failed for non-Foster circuits stability [31]. Therefore, a frequency domain Nyquist stability criterion was proposed for the complete assessment of NFCs [32, 33]. As we know, for a circuit with feedback loop, a pole on the right-half plane (RHP) causes instability. The system of NFC with stability component can be modelled as Fig. 4.12 [34]. It is easy to have the voltage relation as

$$v = \frac{Z_l}{Z_s + Z_l} v_s + \frac{Z_s}{Z_s + Z_l} v_l. \tag{4.7}$$

If Z_s and Z_l are defined as

$$Z_s = \frac{N_s}{D_s}, \tag{4.8}$$

$$Z_l = \frac{N_l}{D_l}, \tag{4.9}$$

Eq. (4.7) can be rewritten as

$$v = \frac{N_l D_s v_s + N_s D_l v_l}{N_l D_s (1 + Z_s Y_l)} \tag{4.10}$$

where $Y_l = 1/Z_l$. In practice, neither N_l nor D_s has RHP zeros [34]. Thus, the circuit is stable if the zeros of $(1 + Z_s Y_l)$ are on the left-half plane (LHP). If we define Z and P as the number of RHP zeros and poles of $(1 + Z_s Y_l)$ respectively, according to Cauchy's
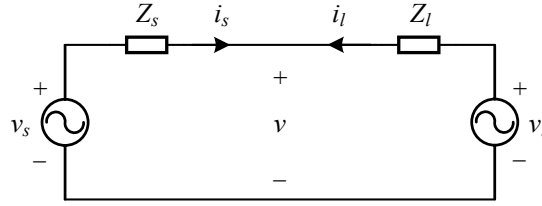
Figure 4.12: Thevenin equivalent source and load converter model.

argument [35] we have

$$N = Z - P, \tag{4.11}$$

As it is often more convenient to explore the product $G(s) = Z_s Y_l$, hence N is the number of clockwise encirclement of point -1 in the complex plot of G(s). In practical systems, neither Z_s nor Y_l has RHP poles [34]. Hence, it is easy to have $N = Z$. For Linvill's OCS system, since the circuit has LHP impedance poles only [27], the stability component (Y_l) is used to stabilise the NFC (Z_s). In practice, it is safe to say a stable circuit must have no net encirclement of -1 point in the contour obtained from the complex plot of G(s). As shown in Fig. 4.13(a), an series connected capacitor C = 10 pF does not stabilize the proposed NFC because the point -1 is encircled. However, when a series capacitor C = 0.5 pF is used. as shown in Fig. 4.13(b), the point -1 is moved out of the net encirclement and the NFC is stabilised.

4.4 NFC Realisation Utilizing Negative Differential Resistance of GFET

As depicted in the last section, the GFET-based Linvill's NFC operates at VHF frequency only. Although the drain current saturation can be improved with thinner gate dielectric, it is still hard to achieve an output resistance comparable to that of BJTs or CMOS transistors. Meanwhile, thinner gate dielectric can result in NDR behaviour that has been experimentally observed, which can potentially degrade the stability performance of the NFC. Hence, the application of this kind of NFC is very limited. As the NFC
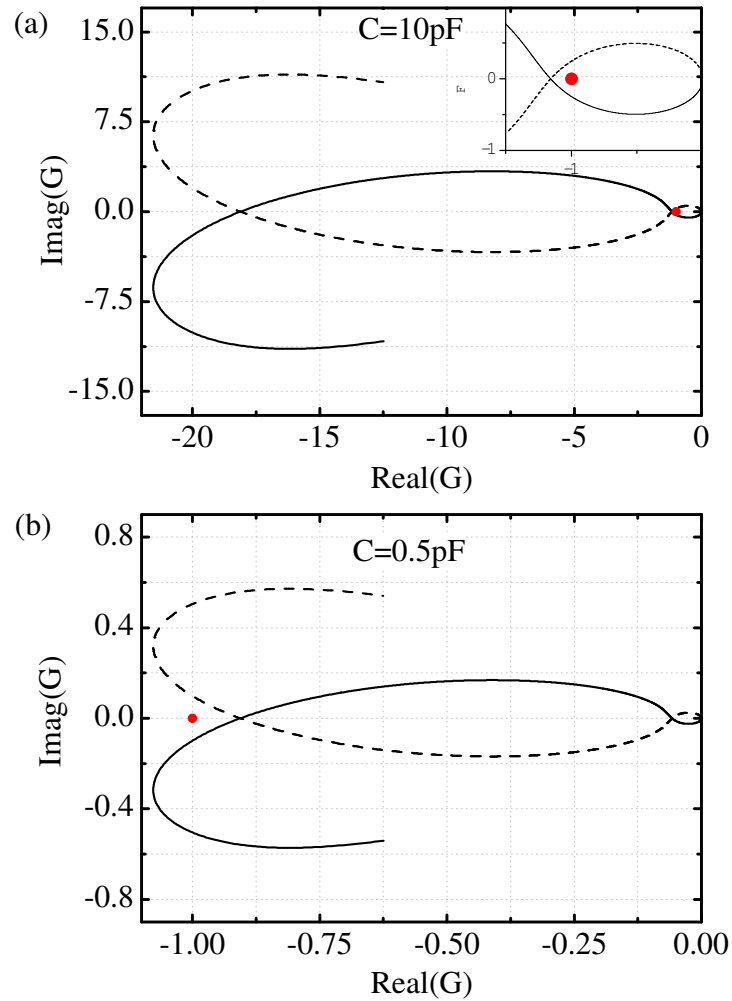
Figure 4.13: Complex plot of G(s) (a) for C = 10 pF (b) for C = 0.5 pF

based on the NDR behaviour of RTD has been successfully demonstrated in [36], in this section, we will explore the use of NDR behaviour of GFET to realise NFC.

4.4.1 Negative Differential Resistance of GFET

In spite of the poor drain current saturation, an interesting property of GFET is its negative differential resistance [37, 38]. Unlike the Si MOSFETs, the carriers in a GFET channel can be either electrons or holes, depending on the gate bias. Under proper bias conditions, the GFET exhibits NDR effect, just like the RTD. In Chapter 2, we have briefly introduced the mechanism behind the NDR phenomenon with a band diagram.

Now, we will look into the details with the results achieved from a drift-diffusion model [38].

As shown in Fig. 4.14(a), the drain current of a 500-nm GFET demonstrates saturation and NDR behaviour at $V_{GS} = -0.5$ V and $V_{GS} = -1$ V, respectively. The corresponding average carrier densities $\langle \rho_{sh} \rangle$ for both gate biases are also depicted in Fig. 4.14(b). It can be seen that $\langle \rho_{sh} \rangle$ is inversely proportional to V_{SD} at small voltages. This is due to the decrease of drain-to-gate voltage when V_{SD} increases, which reduces the carrier density at the drain end. Consequently, the carrier drift velocity v_{drift}, in contrast, increases rapidly with the increase of V_{SD} and eventually saturates at high drain-source bias, as shown in Fig. 4.14(c). Since the drain current is calculated as Eq. (3.8), it is obvious that the NDR phenomenon is caused by the reduction of $\langle \rho_{sh} \rangle$. If we recall the saturation velocity v_{sat} in Eq. (3.47) is carrier density dependent and approximately proportional to $1/\langle \rho_{sh} \rangle$. Hence, it is the competition between the increase of v_{drift} and the decrease of $\langle \rho_{sh} \rangle$ that determines whether the transistor exhibits saturation or NDR behaviour. As shown in Fig. 4.14(b), for both $V_{GS} = -1$ V and $V_{GS} = -0.5$ V, $\langle \rho_{sh} \rangle$ decreases with the same rate when V_{SD} increases. The drift velocity at $V_{GS} = -1$ V is lower than that at $V_{GS} = -0.5$ V, as shown in Fig. 4.14(c), due to the larger $\langle \rho_{sh} \rangle$ at $V_{GS} = -1$. Hence, when $V_{GS} = -0.5$ V, the reduction of $\langle \rho_{sh} \rangle$ and increase of v_{drift} cancel each other near $V_{SD} = 0.5$ V, resulting in close to zero current variation with the increase of V_{SD} (i.e. saturation behaviour). When $V_{GS} = -1$ V, due to the reduced v_{drift}, the decrease of $\langle \rho_{sh} \rangle$ dominates in the resulting drain current and the transistor exhibits NDR behaviour. As shown in Fig. 4.14 (d), the bipolar channel (i.e. part of the channel is electron dominated and the rest is hole dominated) appears when the drain-end carrier density reaches the minimum at $V_{SD} = 1$ V for $V_{GS} = -1$ V. The NDR behaviour, however, starts (at $V_{SD} = 0.86$ V) before the channel enters the bipolar region. Hence, it reveals the NDR behaviour is not caused by the change of carrier types.
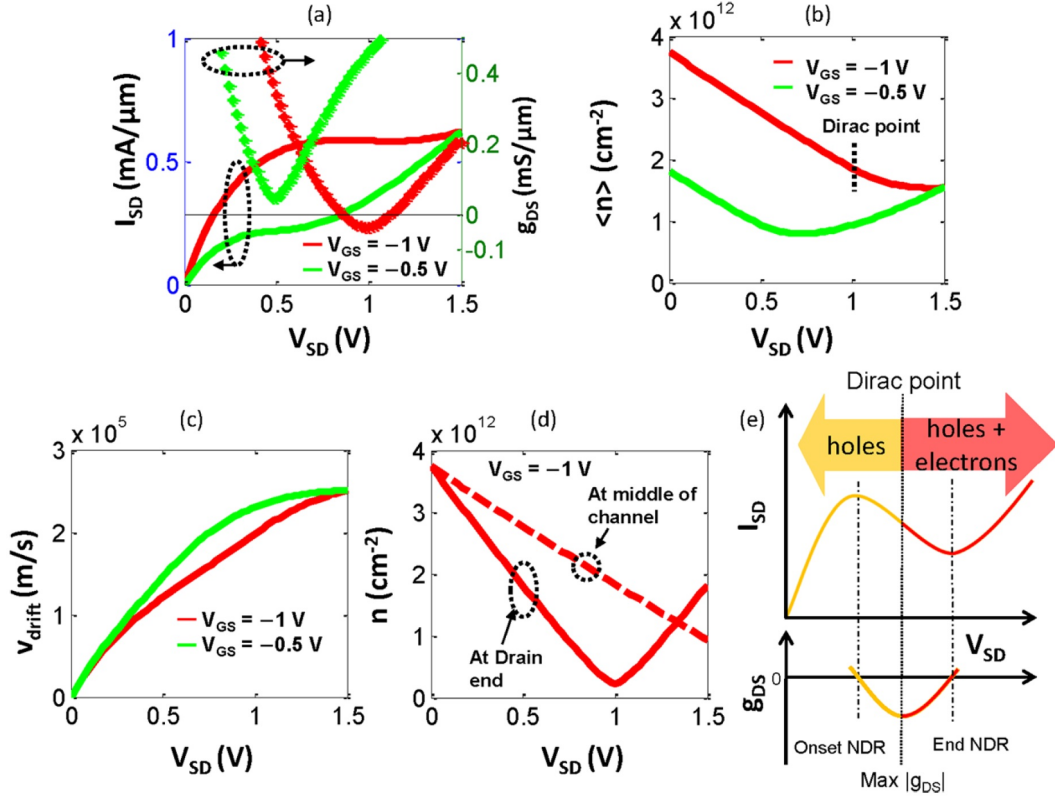
Figure 4.14: Simulated results of a L=500 nm GFET (a) source-to-drain current I_{SD} against source-to-drain voltage for $V_{GS} = -0.5$ V and $V_{GS} = -1$ V; (b) average carrier density $\langle \rho_{sh} \rangle$ as a function of V_{SD} for $V_{GS} = -0.5$ V and $V_{GS} = -1$ V; (c) drift velocity as a function of V_{SD} for $V_{GS} = -0.5$ V and $V_{GS} = -1$ V; (d) charge density as a function of V_{SD} for $V_{GS} = -1$ V; (e) simplified sketch demonstrating the transition from unipolar to bipolar channel [38].

4.4.2 NFC Design

In this section, we explore the feasibility of utilising NDR behaviour of GFET for NFC design. Compared with the double-barrier RTD [36], GFET is less complicated in geometry and the negative resistance can be easily controlled by the channel width-to-length ratio (W/L). This would provide flexibility for the designer to chose the most suitable negative resistance. In addition, as GFETs share the CMOS fabrication process without consuming the silicon area, it is possible to integrate GFET RF/microwave circuits on the top of silicon-based logic circuits. This would significantly reduce the cost of the

overall system. The schematics of series and shunt NFCs based on the NDR of GFET are depicted in Fig. 4.15. Different from Linvill's NFC, the capacitive load in this circuit would result in a negative inductance and vice versa, as shown in Fig. 4.15(a) and (b). The parallel negative RLC tank can also be easily achieved with a series connected RLC load, as shown in Fig. 4.15(c).

The $L = 80\,\mathrm{nm}$ GFET presented in the supporting information of Ref. [37] is used for this NFC design. It is noted that by using the traditional p-doped CVD graphene as channel material, this GFET shows negative resistance at $V_{gs} = 0\,\mathrm{V}$. That implies a diode-connected GFET can be used as the active device without additional gate bias. Thus, less biasing components are needed for the NFC and the circuit diagram is further simplified. As our GFET model is based on the drift-diffusion transport theory which applies only when the channel length is longer than the mean-free-path of graphene, it cannot accurately reproduce the output characteristics of this short-channel GFET. However, since the transistor is connected as a diode in this NFC, all we need is simply a diode model for I_{ds} vs. V_{ds} at $V_{gs} = 0\,\mathrm{V}$ rather than a full GFET model. The relaxed requirement of modelling enables the application of this drift-diffusion based model in our study. From Fig. 4.16 (a) one can see the measured I_{ds} vs. V_{ds} at $V_{gs} = 0\,\mathrm{V}$ is well reproduced with our GFET model. In Fig. 4.16 (b), the modelled output conductance $g_{ds} = dI_{ds}/dV_{ds}$ is also presented, showing excellent matching with the measured results. The GFET channel width $W = 85\,\mu\mathrm{m}$ is carefully calculated to provide an overall negative differential resistance $-R_0 \approx -50\,\Omega$ near the DC bias point $V_{ds} = 1.22\,\mathrm{V}$. According to the relation presented in Fig. 4.15, $-R_0 \approx -50\Omega$ would result in a practical load capacitor or inductor rather than some extremely large or small components. However, R_0 can also be designed to other values according to the application. The same large-signal model of GFET, as shown in Fig. 4.7, is used in this study. The full schematic of the proposed NFC is given as Fig. 4.17.

In order to achieve more accurate results, the EM model of a PCB layout (Fig. 4.18) designed for the proposed NFC is also included for the EM/circuit co-simulation.
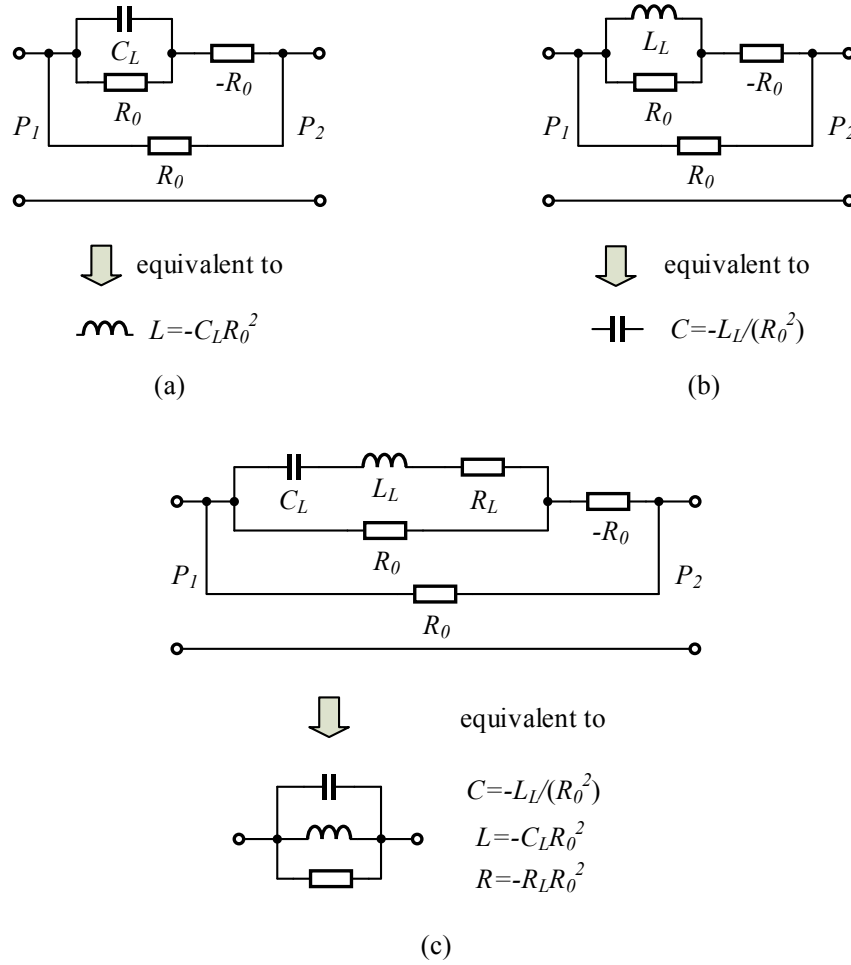
Figure 4.15: Schematic of the proposed NFC (a) negative capacitance, (b) negative inductance and (c) negative shunt RLC.

The DC and RF traces have been designed on the bottom and top layer of the PCB respectively to minimise the unwanted crosstalk issues. The GFET is biased through RF chokes ($L_{choke} = 470\,\text{nH}$) and the RF path is isolated from the DC path by the coupling capacitors ($C_{cp} = 47\,\mu\text{F}$). The NFC prototype is built on 0.8 mm FR-4 substrate, while the footprints of the surface mount RLC devices from Murata library have standard package sizes 0603 or 0805. In Fig. 4.19, the negative capacitance/inductance achieved with the proposed NFC is presented. The device exhibits effective negative capacitance up to 2 GHz and negative inductance up to 1 GHz. This is much better than the GFET-based NFC utilising Linvill's model and is comparable to that of the RTD-based NFC. Compared with Linvill's technique, the design complexity of the proposed NFC are
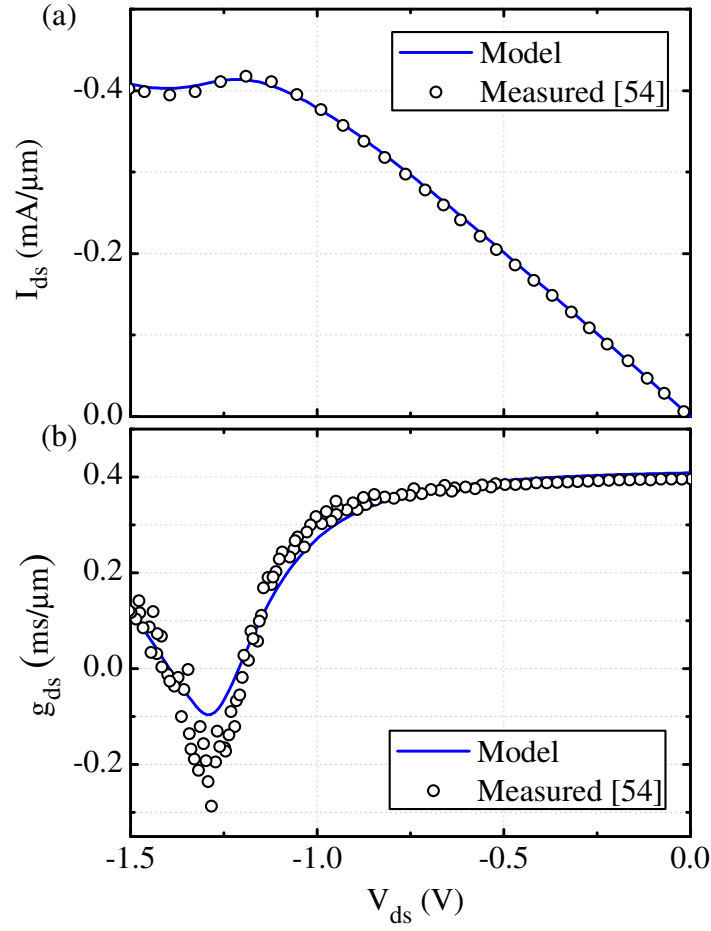
Figure 4.16: Measured and modelled results of $L = 80$nm GFET (a) drain-to-source current I_{ds} and (b) output conductance g_{ds} against V_{ds}. The measured data is provided in the supporting information of [37]. Parameters used in the model: $L = 80$ nm, $t_{oxt} = 1.5$ nm, $k_t = 3.9$, $T = 300$ K, $\mu_p = \mu_n = 5000$ cm^2/Vs, $V_{gs0} = 0.77$ V, $\Delta = 40$ meV, $R_{d/s} = 1.55$ k$\Omega \cdot \mu$m and $m = 1$V^2.
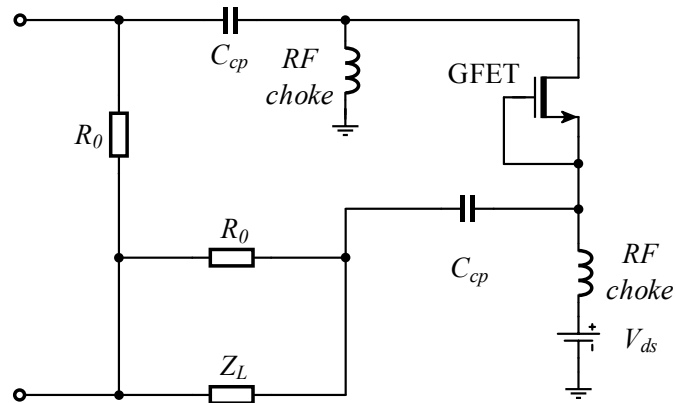
Figure 4.17: Schematic of NDR-based graphene NFC.
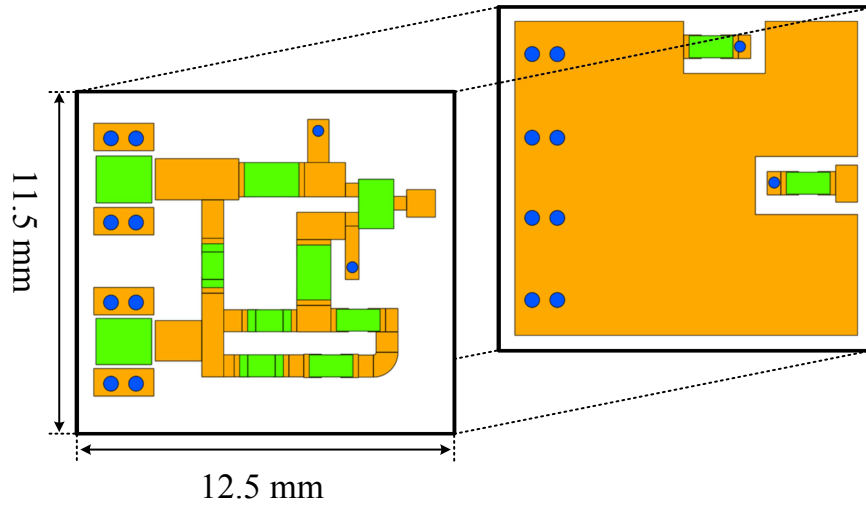
Figure 4.18: Layout including footprint of real components (neglecting the GFET footprint).

highly reduced because of the absence of the positive feedback loop. Therefore, the final layout has a miniaturised dimension of $11.5 \times 12.5\,\mathrm{mm}^2$ only. This low form factor of NFC makes it a potential candidate for applications in metamaterials and metasurfaces. In next chapter, we will investigate the performance of a metasurface loaded with this type of NFCs. The stability of this NFC will be analysed with the presence of the metasurface.

4.5   Conclusion

In conclusion, the feasibility studies of two GFET NFCs utilising different approaches are presented in this chapter. The Verilog-A model of GFET developed in Chapter 3 with estimated parasitics is used as the active element to achieve negative impedance. The EM model of PCB layouts including footprints of real components except GFET has also been taken into account to ensure more realistic results. The Linvill's GFET NFC shows negative capacitance up to 200 MHz and the stability check based on Nyquist stability criterion has been presented. The NFC based on the NDR behaviour of GFET demonstrates improved negative impedance phenomenon up to 2 GHz. Significant NFC
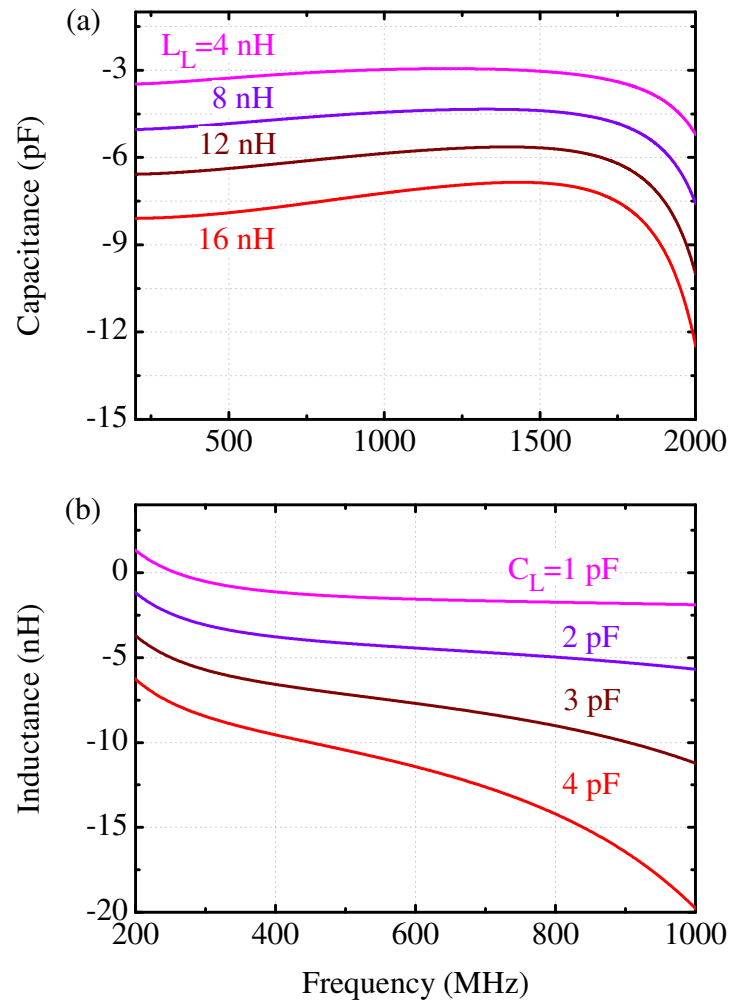
Figure 4.19: Simulations of (a) negative capacitance and (b) inductance for various load conditions.

miniaturization has been achieved through the use of a diode-connected GFET as the active device.

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Chapter 5

High Impedance Surface Loaded with Graphene NFCs

One potentially important application of NFCs is the combination with artificial impedance surfaces to extend the operation bandwidth. The theoretical work has been reported in Ref. [1], followed by a number of publications [2–4] with simulation and measurement results. In this chapter, the simulation results of a high impedance surface (HIS) loaded with the NFCs proposed in section 4.4 are presented. The HISs are usually used as ground planes for compact and low profile antennas, ideally enhancing gain by 3 dB. A typical HIS operates within a narrow region near the center frequency because of the fundamental limitations of the passive resonating structure. Therefore, the NFCs are used to overcome these limitations and achieve broadband operation.

5.1 Conventional Metallic Ground Plane for Antenna

As we know, electric conductors such as metals are good reflectors that can reflect the incident signal but with inverted phase. This is because the electric fields inside the metal is forbidden, thus, according to the law of boundary continuity the tangential

component of the electric field at the metal/air interface is forced to zero. When the electromagnetic wave incident on the metal surface, in order to achieve a node for electric field at the metal surface the reflected wave is forced to be 180 degree out of phase with the incident wave. Consequently, the wave also exhibits an antinode for magnetic field at the interface. For perfect magnetic conductors, it is the other way around that the wave exhibits a node for magnetic field and antinode for electric field at the interface. Thus, a perfect magnetic conductor would reflect the incoming wave in-phase.

For a plane wave reflected at the boundary of a material with surface impedance of Z_s, the reflection coefficient for electric field can be written as

$$\Gamma = \frac{Z_s - \eta_0}{Z_s + \eta_0}, \tag{5.1}$$

where $\eta_0 = 377\,\Omega$ is the characteristic impedance of free space. For good conductors like metal $Z_s \approx 0$, it is easy to achieve $\Gamma = -1$. Hence, the reflected signal is out of phase. To achieve in-phase reflection, from Eq. (5.1) it is easy to see the condition is $Z_s \to \infty$. Therefore, the magnetic conductors, that only exists mathematically, has infinite surface impedance.

In many applications, metallic (or perfect electric conductor (PEC)) sheets are used as ground planes or reflectors to improve the directivity of antenna. Ideally, if the radiated and reflected signals are in phase, this topology would improve the antenna gain by 3 dB while providing certain shielding to reduce the interference on the other side of the reflector. However, if the antenna is placed too close to the ground plane, as shown in Fig. 5.1, the ground plane reflects the signal out of phase, causing unwanted cancelling between the radiated and reflected waves. Hence, the antenna is virtually shorted out and the strength of radiation signal is significantly decreased. In order to maximize the gain, the ground plane has to be placed precisely at a distance of $(1/4 + n)\lambda$ $(n = 0, 1, 2, 3 \cdots)$ from the antenna, as shown in Fig. 5.2, where λ is the wavelength of the incident signal. This placement leads to an overall $2(n+1)\pi$ phase shift to the reflected wave so that the
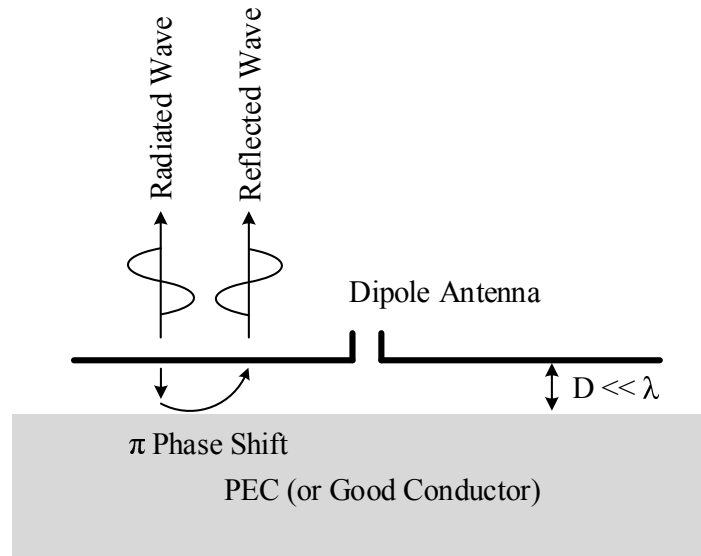
Figure 5.1: Out-of-phase reflection when the antenna is placed close to the ground plane.
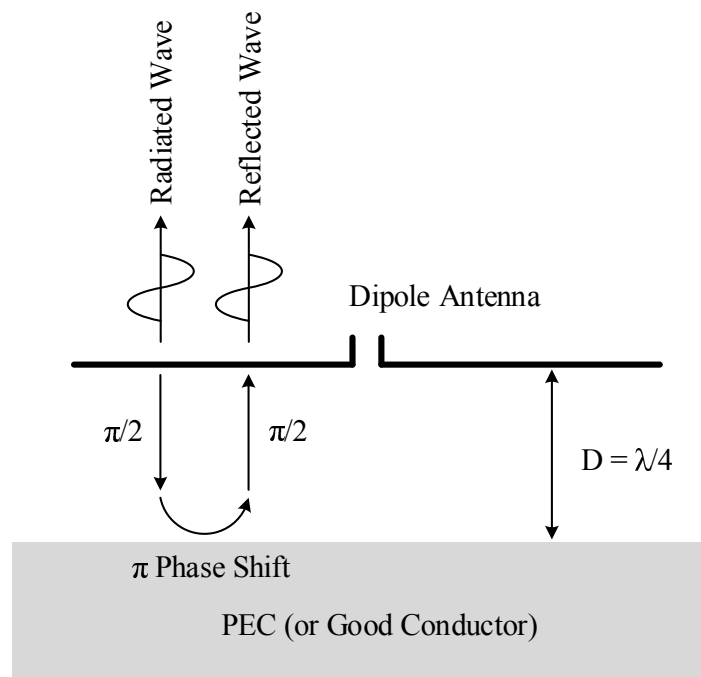
Figure 5.2: In-phase reflection when the antenna is placed at a distance of $\lambda/4$ from ground plane.

reflected and radiated waves are in-phase now, which improves the antenna gain by 3dB. It is noted this topology requires a thickness of at least $\lambda/4$ that is not easy to achieve in practice. Meanwhile, metal supports the propagation of surface waves that are bound to

the metal/air interface. At optical frequencies these waves are called surface plasmons which is strictly localized at the metal surface but at microwave frequencies they are just AC currents that exist up to thousands of wavelengths into the metal. The surface waves do not couple to external plane waves on smooth and flat metal but would radiate if they are scattered by bends or discontinuities. Hence, they are not desired at many applications. For example, if an antenna is placed close to a metal ground plane, the surface wave generated by the radiated signal would propagate along the sheet. For a flat and infinite large metal sheet this surface wave would not cause any effect to the antenna performance except a slight radiation efficiency reduction. However, in practice the bends and finite size of the ground plane would lead to radiation of surface waves, resulting in multipath interference. In addition, if the ground plane is shared by several antennas, mutual coupling would occur due to the propagation of surface waves.

5.2 High Impedance Surface

HIS, also known as high impedance ground plane or artificial magnetic conductor, is a kind of metallic metasurface that performs as magnetic wall over a pre-designed bandwidth. It is basically a periodic metal patch or strip array as shown in Fig. 5.3, exhibiting similar performance as resonators to prevent electric current conduction. Although HIS conducts DC current, the unique geometry of this metamaterial stops it from conducting AC current within a forbidden frequency range, enabling the suppression of surface waves over these frequencies. The potential applications of HIS such as antenna radiation enhancement and artificial dielectrics has been widely discussed in [5–16]. When the patch size is much smaller than the wavelength, the electromagnetic property of a HIS can be modelled with lumped LC components, as shown in Fig. 5.4. The capacitances are originated from the coupling between adjacent elements while the physical path between the patches provides the inductance. At the frequency of infinite surface impedance, the tangential component of magnetic field on the HIS surface is zero

(a)

(b)
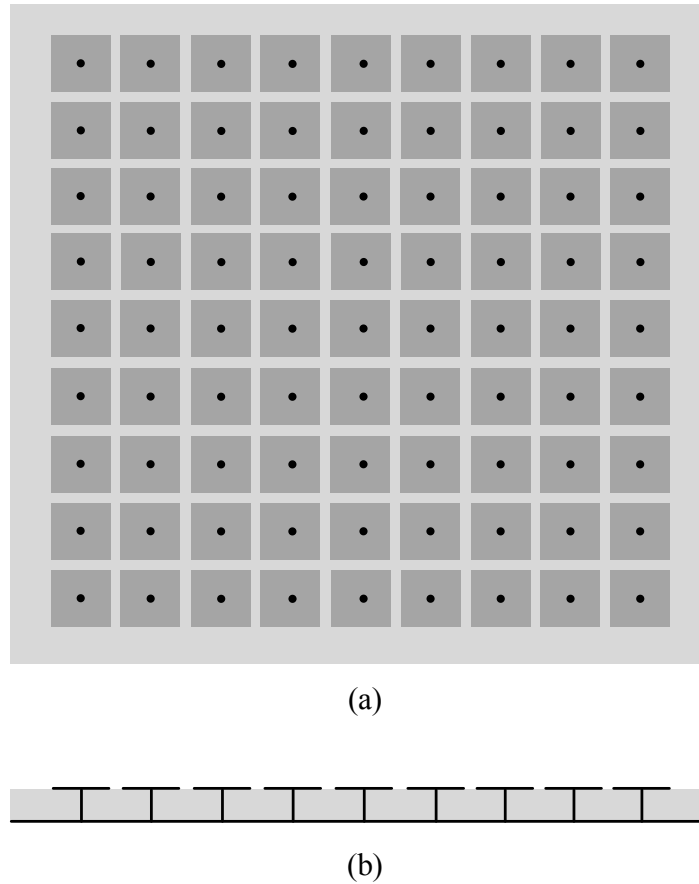
Figure 5.3: Schematic of high impedance surface (a) top view and (b) cross-sectional view.
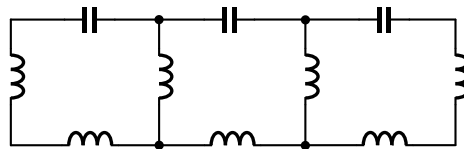
Figure 5.4: Ideal equivalent circuit model of high impedance surface.

regardless the strength of electric field. Hence, the HIS is able to reflect the incident wave without phase reversal over its operation bandwidth, as shown in Fig 5.5.

It has been discussed in [17] that in order to enhance the gain of the antenna, the phase of the reflection coefficient has to stay between $+\pi/2$ and $-\pi/2$. Out of this region, the HIS provides loss rather than gain to the antenna. The theoretical bounds of the HIS bandwidth has been reported in [18]. Typically, the bandwidth can be improved by increasing the thickness of the substrate. However, this in not practical in applications
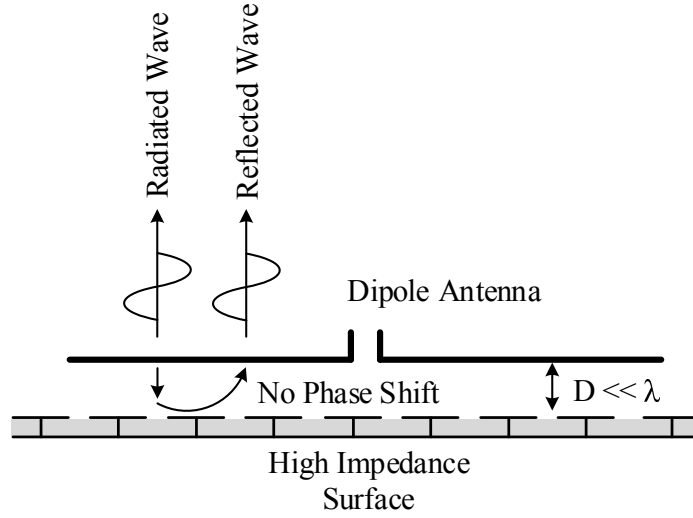
Figure 5.5: In-phase reflection when the antenna is placed close to a high impedance surface.

such as portable devices where only limited space is allowed for the antenna placement. Therefore, the idea of connecting NFCs with HIS to extend the operation bandwidth was proposed [3, 19].

5.3 Effective Medium Model of HIS

The equivalent circuit model, as shown in Fig. 5.6, can be used to simulate the performance of HIS [20]. The metallic patch array is modelled as the grid impedance consisting of parallel connected conductance G and capacitance C. The metallic wires are modelled as the surface impedance composed of series connected L_s and R_s.

5.3.1 Grid Impedance

For the periodic metallic strip array as shown in Fig. 5.7, if the strip width is much smaller than the period D (i.e. $w << D$), the array can be assumed as nearly isotropic that its electromagnetic response is nearly independent of the plane of incidence. Hence, once the grid impedance of incidence in xz plane (z axis is perpendicular to the xy plane)
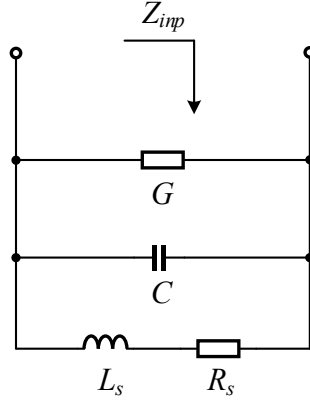
Figure 5.6: Non-ideal equivalent circuit model of high impedance surface with grid conductance G and series resistance R_s.
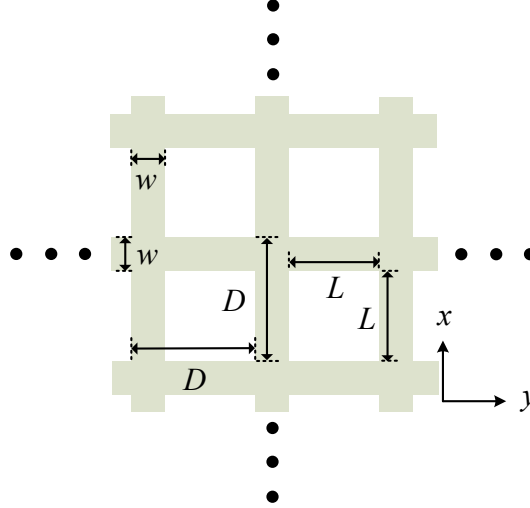
Figure 5.7: Schematic of the periodic metallic strip array.

is derived, it would be also valid for arbitrary incidence plane. The grid impedance is defined as the ratio between averaged tangential electric field in the grid plane $\vec{E}_y$ (or $\vec{E}_x$) and the averaged surface current density $\vec{J}_y$ (or $\vec{J}_x$) induced by the incident wave:

$$Z_{g'}^{TE} = \frac{\vec{E}_y}{\vec{J}_y}, \tag{5.2}$$

$$Z_{g'}^{TM} = \frac{\vec{E}_x}{\vec{J}_x}, \tag{5.3}$$

where $Z_{g'}^{TE}$ and $Z_{g'}^{TM}$ are the grid impedance for TE- and TM-polarized waves respectively. The averaged tangential electric fields for TE- and TM-polarized waves have been

derived as [21]

$$\vec{E}_y = j\frac{\eta_{eff}}{2}\alpha_d\vec{J}_y, \tag{5.4}$$

$$\vec{E}_x = j\frac{\eta_{eff}}{2}\alpha_d\left[\vec{J}_x + \frac{1}{k_{eff}^2\left(1+\dfrac{b}{D}\right)}\frac{b}{D}\frac{\partial^2}{\partial x^2}\vec{J}_x\right], \tag{5.5}$$

where b and D are the periods in x and y direction, respectively. For square patch array one have $b = D$. $\eta_{eff} = \sqrt{\mu_0/\epsilon_0\epsilon_{eff}}$ is the effective wave impedance of the host medium and

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} \tag{5.6}$$

is the effective permittivity. $k_{eff} = k_0\sqrt{\epsilon_{eff}}$ is the incident wave number in host medium. ϵ_0, μ_0 and k_0 are free space permittivity, permittivity and wave number respectively. α_d is the grid parameter for electrically dense array of metallic strips

$$\alpha_d = \frac{k_{eff}D}{\pi}\ln\left(\frac{1}{\sin\dfrac{\pi\omega}{2D}}\right), \tag{5.7}$$

where w is the strip width. By substituting $(\partial)/(\partial x)$ with $-jk_x$ in Eq. (5.5), where $k_x = k_0\sin\theta$ is the x-component of the incident wave vector in free space and θ is the incidence angle, the grid impedance can be rewritten as

$$Z_{g'}^{TM} = -j\frac{\eta_{eff}}{2}\alpha_d\left(1 - \frac{k_0^2\sin^2\theta}{2k_{eff}^2}\right). \tag{5.8}$$

On the other hand, the grid impedance of TE-polarized wave can be achieved by substituting Eq. (5.4) into (5.2)

$$Z_{g'}^{TE} = -j\frac{\eta_{eff}}{2}\alpha_d. \tag{5.9}$$

According to the approximate Babinet principle [22, 23], the follow relations exist

$$Z_g^{TE} Z_{g'}^{TM} = \frac{\eta_{eff}^2}{4}, \tag{5.10}$$

$$Z_{g'}^{TE} Z_g^{TM} = \frac{\eta_{eff}^2}{4}, \tag{5.11}$$

where Z_g^{TE} and Z_g^{TM} are the grid impedance for the TE and TM-polarized incident waves of the complementary structure, as shown in Fig. 5.8. Hence, the grid impedance of the metallic patch array are [24]

$$Z_g^{TE} = -j\frac{\eta_{eff}}{2\alpha_d \left(1 - \dfrac{k_0^2 \sin^2 \theta}{2k_{eff}^2}\right)}, \tag{5.12}$$

$$Z_g^{TM} = -j\frac{\eta_{eff}}{2\alpha_d}. \tag{5.13}$$

For normal incidence where $\theta = 0$, the grid impedance for TE and TM-polarized incident wave are identical:

$$Z_g^{TE,TM} = -j\frac{\eta_{eff}}{2\alpha_d}. \tag{5.14}$$

It is easy to see that from Eq. (5.14) the grid impedance seems purely capacitive. However, for lossy substrate, the complex permittivity should be used

$$\epsilon_r = \epsilon_r' - j\epsilon_r'' = \epsilon_r'\left(1 - j\tan\delta\right), \tag{5.15}$$

and the grid impedance would have the following form

$$Z_g^{TE,TM} = \frac{1}{G + j\omega C}. \tag{5.16}$$

Substituting (5.6), (5.7) and Eq. (5.15) into (5.14), the equivalent lumped elements
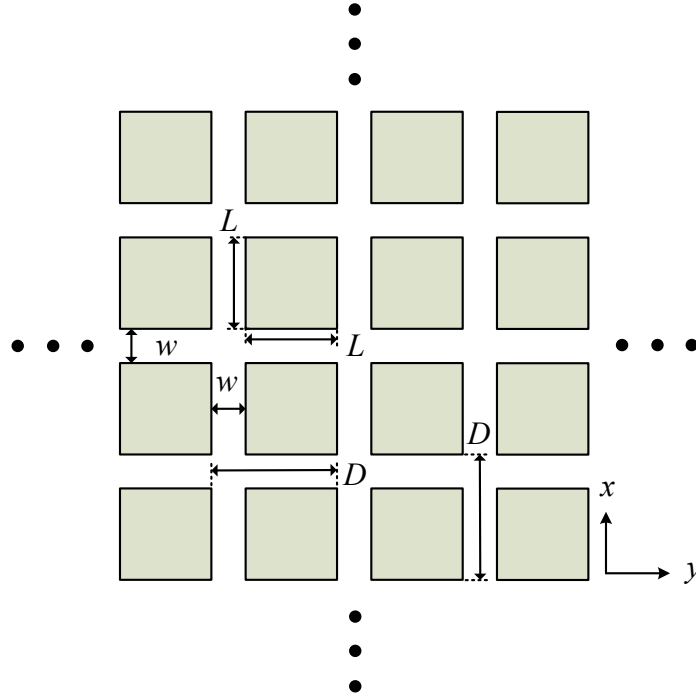
Figure 5.8: Metallic patch array as the complementary structure of the periodic strip array.

of the grid impedance for normal incidence can be derived as [20]

$$C = -\frac{D\epsilon_0 \left(\epsilon_r' + 1 \right)}{\pi} \ln \left(\frac{1}{\sin \left(\frac{\pi\omega}{2D} \right)} \right), \tag{5.17}$$

$$G = -\frac{\omega D\epsilon_0 \epsilon_r''}{\pi} \ln \left(\frac{1}{\sin \left(\frac{\pi\omega}{2D} \right)} \right). \tag{5.18}$$

5.3.2 Surface Impedance

The surface impedance of a wire medium consists of metallic wire array and substrate with dielectric constant ϵ_r, as shown in Fig. 5.9, has been derived as [23, 24]

$$Z_s^{TE} = j\omega\mu_0 \frac{\tan \left(k_y d \right)}{k_y}, \tag{5.19}$$
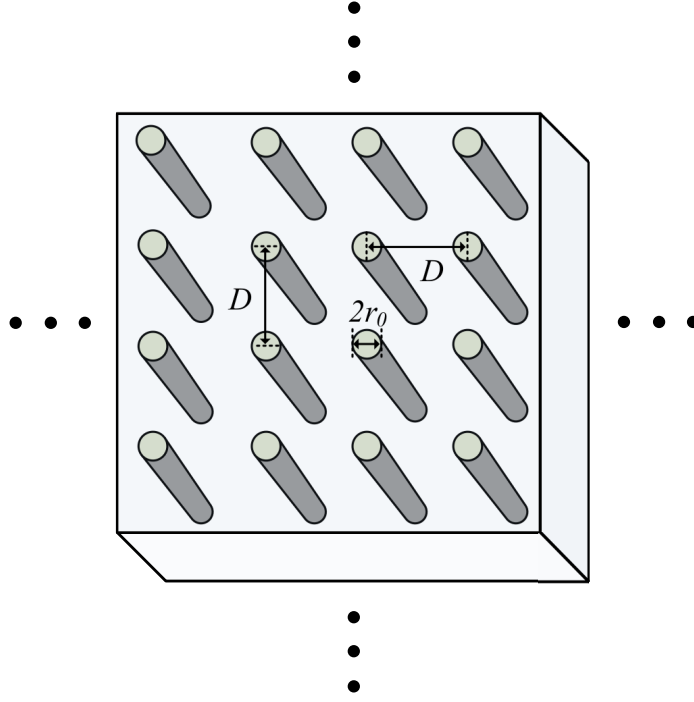
Figure 5.9: Schematic of dielectric surrounded metallic via array.

$$Z_s^{TM} = j\omega\mu_0 \frac{\tan(\gamma_{TM}d)}{\gamma_{TM}} \frac{k^2 - \beta^2 - k_p^2}{k^2 - k_p^2}, \tag{5.20}$$

where Z_s^{TE} and Z_s^{TM} are the surface impedance of TE and TM-polarized wave respectively. $k = k_0\sqrt{\epsilon_r}$ is the number of wave in the host medium. $\beta = \pm\sqrt{k^2 - k_y^2}$ and $k_y = k\cos(\theta)$ is the tangential component of the wave number imposed by the incident wave. The expressions of γ_{TM}^2 and k_p are given as below

$$\gamma_{TM}^2 = \omega^2 \epsilon_0 \epsilon_t \mu_0 - \frac{\epsilon_t}{\epsilon_n}\beta^2, \tag{5.21}$$

$$k_p = \frac{1}{D\sqrt{\dfrac{1}{2\pi}\ln\dfrac{D^2}{4r_0(D-r_0)}}}, \tag{5.22}$$

where ϵ_t is the relative permittivity for the fields along the transverse plane, which equals to ϵ_r if the vias are thin and vertically placed. r_0 is the via radius and ϵ_n is the relative

permittivity for the fields along the normal of the medium with the following expression

$$\epsilon_n = \epsilon_t \left(1 - \frac{k_p^2}{k^2 \epsilon_t} \right). \tag{5.23}$$

For normal incidence, one have $\theta = 0$ and the identical expression of Z_s is achieved for TE- and TM-polarized waves as [20]

$$Z_s^{TE,TM} = j\omega\mu_0 \frac{\tan(kd)}{k}, \tag{5.24}$$

and the inductance can be calculated as

$$L_s^{TE,TM} = \frac{Z_s^{TE,TM}}{j\omega} = \mu_0 \frac{\tan(kd)}{k}. \tag{5.25}$$

In the case of lossy medium, the surface impedance should be written as

$$Z_s^{TE,TM} = R_s + j\omega L_s \tag{5.26}$$

Again, by substituting Eq. (5.15) into (5.24), after simplification yielding [20]

$$L_s = \frac{\mu_0 d \sqrt{\sin^2 x + \sinh^2 y}}{\sqrt{\cos^2 x + \sinh^2 y} \sqrt{x^2 + y^2}} \cos \left[\tan^{-1} \left(\frac{\sinh(2y)}{\sin(2x)} \right) - \tan^{-1} \left(\frac{y}{x} \right) \right], \tag{5.27}$$

$$R_s = \frac{\omega\mu_0 d \sqrt{\sin^2 x + \sinh^2 y}}{\sqrt{\cos^2 x + \sinh^2 y} \sqrt{x^2 + y^2}} \sin \left[\tan^{-1} \left(\frac{\sinh(2y)}{\sin(2x)} \right) - \tan^{-1} \left(\frac{y}{x} \right) \right], \tag{5.28}$$

where

$$x = k_0 d \sqrt{\frac{\epsilon_r'}{\cos\delta}} \cos\frac{\delta}{2}, \tag{5.29}$$

$$y = k_0 d \sqrt{\frac{\epsilon_r'}{\cos\delta}} \sin\frac{\delta}{2}. \tag{5.30}$$

Fig. 5.10 illustrates the corresponding grid impedance and surface impedance components as functions of frequency. The corresponding HIS has dimensions of D = 90 mm,
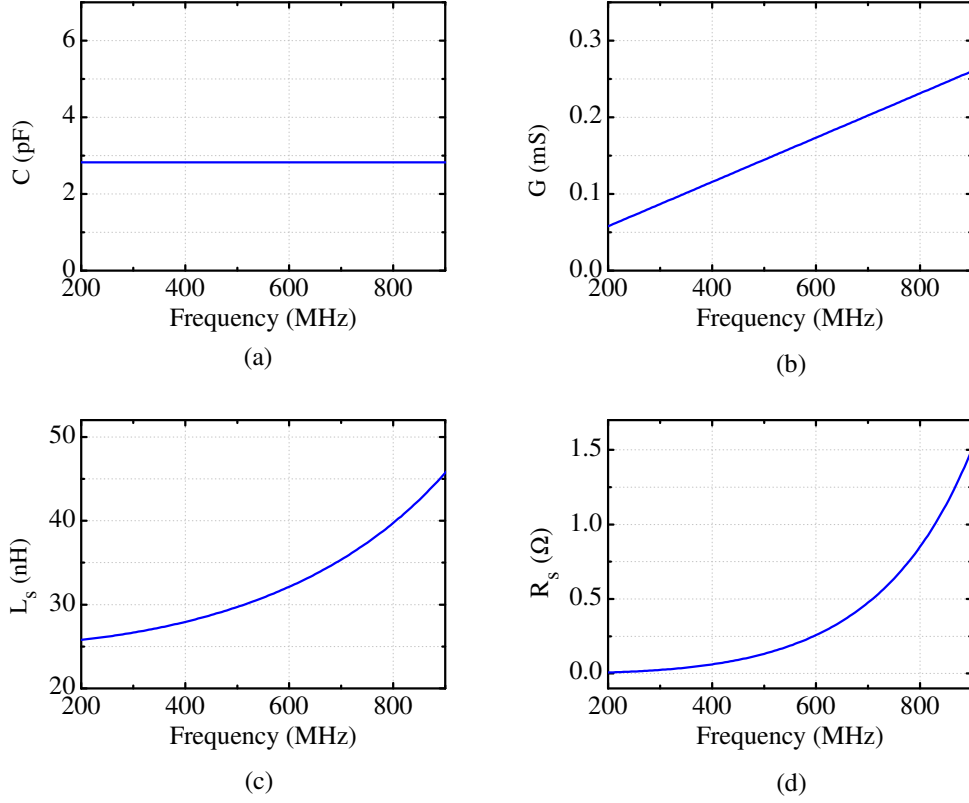
Figure 5.10: Plot of (a) grid capacitance (b) grid conductance (c) surface inductance (d) surface resistance as functions of frequency.

w = 10 mm and d = 20 mm. The dielectric constant and loss tangent of the substrate are 4.4 and 0.02 respectively.

5.3.3   Reflection Coefficient

The reflection coefficient can be calculated with the equivalent circuit model. The equivalent input impedance of the circuit shown in Fig. 5.6 is [20]

$$Z_{inp} = \left(Z_g^{-1} + Z_s^{-1}\right)^{-1} = \frac{R_s + j\omega L_s}{1 + R_s G + j\omega\left(L_s G + C R_s\right) - \omega^2 L_s C}, \tag{5.31}$$

where C, g, L_s and R_s are equivalent lumped elements derived in the previous section. Thus, the reflection coefficient is calculated as

$$\Gamma = \frac{Z_{inp} - \eta_0}{Z_{inp} + \eta_0} \tag{5.32}$$

The resonance frequency of HIS can be extracted from the pole of Z_{inp}

$$1 + R_s G + j\omega \left(L_s G + C R_s \right) - \omega_0^2 L_s C \approx 1 - \omega_0^2 L_s C = 0, \tag{5.33}$$

Hence,

$$\omega_0 = \sqrt{\frac{1}{L_{s0} C}}, \tag{5.34}$$

where L_{s0} is the inductance at the resonant frequency.

The bandwidth of HIS can be approximated as [20]

$$\text{BW} = \frac{\Delta\omega}{\omega_0} = \frac{1}{\eta_0}\sqrt{\frac{L_{s0}}{C}}, \tag{5.35}$$

It is easy to see the bandwidth can be improved by increasing L_{s0} or decreasing C.

In this thesis, the reflection coefficient (S_{11}) of the HIS is calculated with both the equivalent circuit model (ECM) and numerical simulations for crosschecking. As shown in Fig. 5.11, both calculations give the same center frequency of around 540 MHz. Hence, the validation of the ECM is confirmed.

5.4   High Impedance Surface Loaded with NFC

As shown in Fig. 5.11, a typical HIS operates within a narrow region near the center frequency because of the fundamental limitations of the passive resonating structure. It is not practical to increase L_{s0} or decrease C for bandwidth extension. Therefore, the idea of actively-loaded HIS is proposed to achieve broader bandwidth. Since the GFET-based
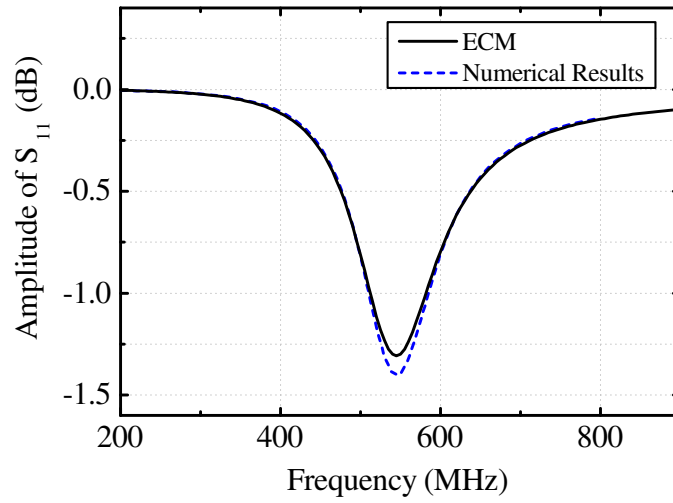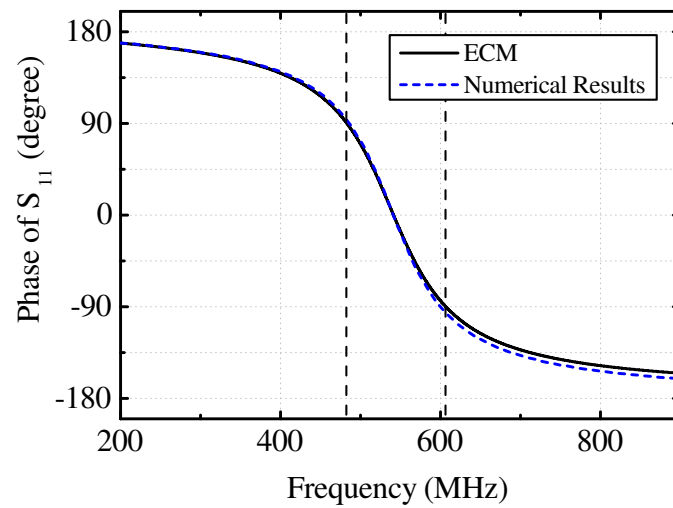
Figure 5.11: Plot of S_{11} against frequency (a) magnitude (b) phase.

Linvill's NFC only operates at VHF band, in this work we have chosen the NDR-based NFC shown in Fig. 4.15, which is able to operate up to 2 GHz. The circuit consists of a GFET biased at the NDR region and a series connected RLC tank. Ideally, the resultant equivalent circuit is a shunt negative RLC. With the floating NFCs connected between adjacent patches, as shown in Fig. 5.12, the new schematic and ECM can be depicted as Fig. 5.13. The overall inductance and capacitance can be approximated as (neglecting
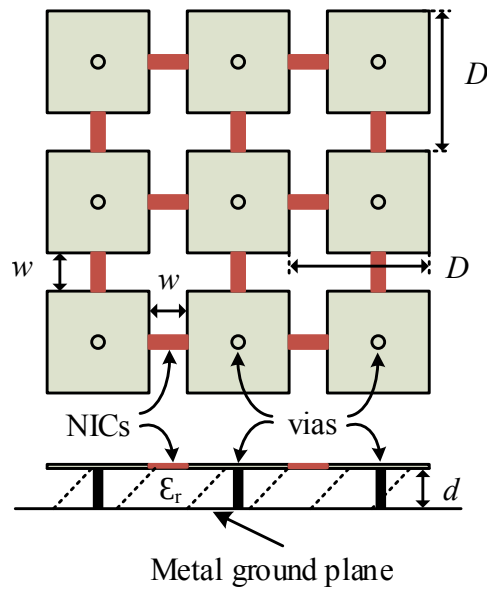
Figure 5.12: Schematic of NFCs loaded high impedance surface

(a)

(b)
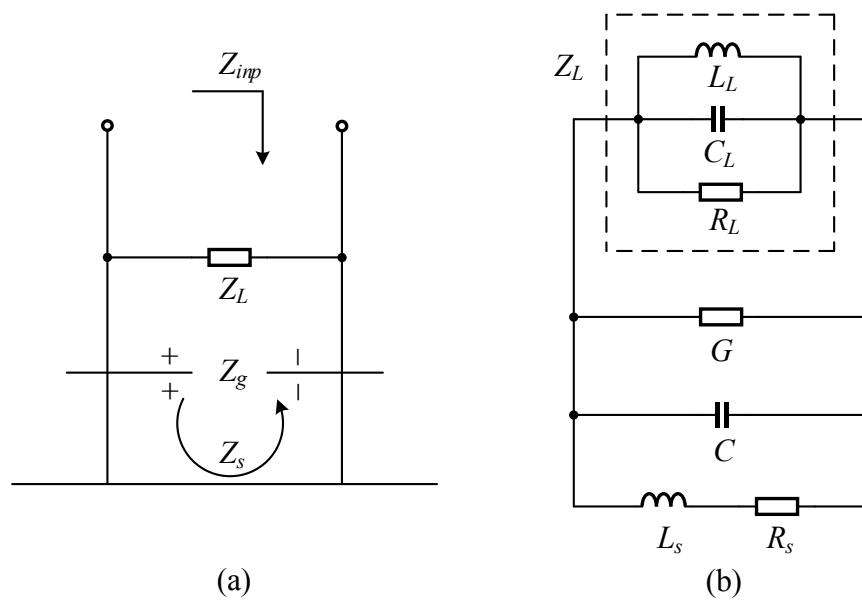
Figure 5.13: High impedance surface loaded with NFCs (a) cross-sectional schematic (b) equivalent circuit model.

R_s and G)

$$L_{HIS} = \frac{L_s L_L}{L_s + L_L},\qquad(5.36)$$

and

$$C_{HIS} = C + C_L.\qquad(5.37)$$

Hence, the fractional bandwidth, which is proportional to $\sqrt{L_{HIS}/C_{HIS}}$, becomes infinite at the extreme limit $L_L = -L_s$ and $C_L = -C$. In practice, the maximum bandwidth enhancement is limited by the operation bandwidth of the NFC.

5.4.1 Stability Characterization

Although it is shown mathematically that infinite bandwidth can be achieved for actively-loaded HIS, in practice the stability requirements do not allow the implementation of such NFCs. To understand the requirement of avoiding NFCs oscillation, the Routh-Hurwitz method is used here for stability analysis [25, 26]. The results of this approach has been validated against the Nyquist stability criterion used in Chapter 4 [20]. The advantage of Routh-Hurwitz method is it gives the analytical expression of the boundary conditions for stability analysis.

Assume the impedance of the close-loop circuit in Fig. 5.13 is [20]

$$Z(s) = \frac{Z_n(s)}{Z_d(s)} = Z_0(s) + Z_L(s) = Z_g(s)\|Z_s(s) + Z_L(s) \tag{5.38}$$

where

$$Z_0(s) = Z_g(s)\|Z_s(s) = \left(\frac{1}{sC} + R + \frac{1}{R_s + sL_s}\right)^{-1} \tag{5.39}$$

is the impedance of the passive HIS and

$$Z_L(s) = \left(\frac{1}{sL_L} + \frac{1}{R_L} + sC_L\right)^{-1} \tag{5.40}$$

is the impedance of NFC. Substitute Eq. (5.39) and (5.40) into (5.38), the numerator of $Z(s)$ can be derived as

$$Z_n(s) = \sum_{k=0}^{K} a_k s^k \tag{5.41}$$

where the coefficients are

$$a_0 = RR_LR_s, \tag{5.42}$$

$$a_1 = RL_sR_L + L_L(RR_s + R_LR_s + R_LR), \qquad (5.43)$$

$$a_2 = L_L\left[L_s\left(R + R_L\right) + RR_LR_s\left(C + C_L\right)\right], \qquad (5.44)$$

$$a_3 = L_LL_sRR_L(C + C_L). \qquad (5.45)$$

$R = 1/G$ is the grid resistance. The system is stable if the zeros of $Z(s)$ are all in the LHP. According to the Routh-Hurwitz criterion, the roots of $Z_n(s) = 0$ are in the LHP if the conditions $a_0/a_3 > 0$, $a_2/a_3 > 0$ and $a_2a_1 > a_0a_3$ are matched. Hence, it is easy to achieve the following condition for stable HIS

$$C_L < -C \qquad (5.46)$$

$$- R < R_L < -\frac{RR_s}{R + R_s} \qquad (5.47)$$

$$- L_s \approx -\frac{RL_sR_L}{RR_s + R_LR_s + R_LR} < L_L < 0 \qquad (5.48)$$

5.4.2 Demonstration of Bandwidth Extension

As introduced before, the bandwidth of HIS is determined between ±90 degree of the phase of S_{11}. According to the stability bounds derived in the last section, in order to achieve stable NFCs a shunt negative RLC combination of $R_L = -450\,\Omega$, $L_L = -20\,\text{nH}$ and $C_L = -4.33\,\text{pF}$ is chosen as the NFC load. The results of graphene-NFC-loaded HIS is also compared with a HIS loaded with ideal -RLC components. From the blue lines of Fig. 5.14, it can be seen that both simulations achieve comparable performance within the frequencies of interest. The bandwidth of HIS is increased from 23% to 54.6%. It is noted the phase characteristic is flipped compared with the unloaded case and actively-loaded HISs in [1] and [3]. This is because the stability condition is not considered in [1] and the HIS loaded with a single negative-L in [3] has different stability requirement $(-L < -L_s)$ from our work. As the purpose of HIS is just to reflect the incident wave in phase (i.e. within ±90°), this flipped phase behaviour does not affect the overall
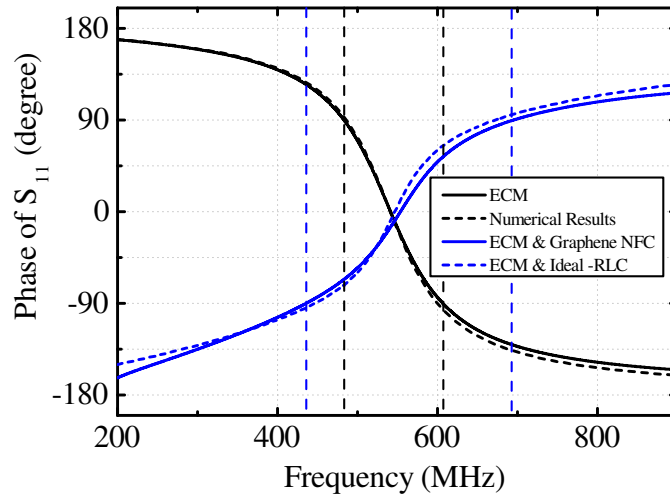
Figure 5.14: Phase of S_{11} against frequency. Black lines are for passive HIS and blue lines are for actively-loaded HIS.

performance of our HIS. In addition, it is worth mentioning that the stability bounds used in this work is derived with ideal -RLC, hence, extra care has to be taken to avoid oscillation as the actual stability bounds may vary due to the parasitics of the graphene NFCs.

5.4.3 Conclusion

In this chapter, the concept of using HIS for gain improvement of low-profile antenna is briefly introduced. The derivation of ECM of HIS has also been presented and results from numerical simulation have been used to validate the ECM. The derivation of stability bounds using Routh-Hurwitz method is also discussed. The bandwidth improvement of an actively-loaded HIS using the graphene NFC proposed in Chapter 4 has also been demonstrated. The simulation results show a bandwidth improvement from 23% to 54.6%. It is also worth noting that while NFC enhances the bandwidth of HIS, the complexity and cost of the actively-loaded system also increases drastically. Hence, NFCs are most likely used in those low profile antennas where the cost of product is a secondary consideration. In addition, the utilization of active NFC circuits increases the energy consumption of the overall system. Moreover, as an active circuit NFC may also

introduce extra noise to the reflected signal, which can reduce the signal-to-noise ratio of the overall radiated wave. The noise analysis of actively-loaded HIS needs further exploration.

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Chapter 6

Conclusion and Future Work

In this chapter, the work presented in this thesis is summarised and a few ideas for the future research are also proposed.

6.1   Conclusion

As the first isolated 2D material, graphene with extraordinary electronic properties has been of great interest to the development of novel electronic devices. In this thesis the theory, modelling and implementation of GFET have been presented.

An overview of researches in 2D materials as well as the concept of non-Foster circuit is introduced in **Chapter 1**. **Chapter 2** provides a review on the properties and synthesis of graphene alongside with the current status of graphene transistors. The ultrahigh carrier mobility of graphene beyond that of any other known materials makes GFET very promising for high speed transistors. The mechanically exfoliated graphene shows the highest carrier mobility among all synthesis approaches and the epitaxial graphene exhibits better sample quality than the CVD grown counterpart. Due to the low cost and high yield of CVD graphene, it has been popular in the fabrication of proof-of-concept devices. The nature of zero bandgap in graphene leads to low on-off ratio and the lack

of drain current saturation in GFETs. The utilisation of thin gate dielectric improves GFET's output resistance because of the increase in the drop rate of average channel charge density. Bandgap engineering of graphene is also available through width control of arm-chaired GNR or applying vertical bias to bilayer graphene. The graphene-based vertical tunnelling transistors utilising MoS_2 and WS_2 as tunnelling barriers demonstrate high on-off current ratio for logic applications. The HETs with graphene base exhibit excellent saturation current and a high on-off ratio of 10^5. However, the mechanism behind the low transfer ratio of graphene HETs are still not fully understood.

Chapter 3 depicts the modelling of graphene transistors. The concept of multiscale modelling is introduced. The *ab initio* and atomistic modelling are suitable for the performance prediction of atomic-scale devices and the semiclassical device modelling is used to model relatively large transistors. Circuit simulation requires the implementation of analytical models. A novel GFET model based on the drift-diffusion transport theory is derived. The modelling aspects including charge density, quantum capacitance, effective carrier mobility and saturation velocity are conducted. The Verilog-A algorithm is used to solve the channel potential at drain and source end automatically and the analytical expression of the drain current is derived based on the modelling aspects. The model is validated against numerical calculation and measurement results and a detailed comparison of existing GFET models is presented at the end.

Chapter 4 illustrates the analog/RF implementation of the GFET. An overview of graphene RF circuits including frequency doubler, mixer, amplifier and oscillator is presented. The ambipolar conduction of GFET enables the realisation of single-transistor frequency doubler and mixer. The GFET subharmonic mixer is favoured for millimetre wavelengths applications as a powerful LO source not available at this frequency. The passive GFET mixer consumes zero DC power and exhibits high linearity performance. The triple-mode GFET amplifier demonstrates the ability to simplify the circuit of PSK and FSK regardless of its low voltage gain. The design of NFCs with GFET is explored through circuit simulation with the model derived in Chapter 3. The history and h-

model of NFC is also presented and two different approaches are introduced to realise GFET NFCs. The first approach is based on the Linvill's technique which uses a pair of cross-coupled GFET as the active circuit. Due to the poor RF performance of GFET, this NFC demonstrates negative impedance at VHF frequency. The second method utilises a diode-connected GFET with negative resistance to achieve NFC. The circuit demonstrates negative impedance up to 2 GHz. The stability analysis of NFC is also conducted.

Chapter 5 presents the bandwidth extension of high impedance surface with graphene NFCs. The equivalent circuit model of HIS composed of grid and surface impedances are presented and the stability analysis of actively-loaded HIS is illustrated with the Routh-Hurwitz method. The simulation results of NDR based graphene NFC are used to demonstrate the bandwidth improvement of HIS.

The main contributions of this thesis are summarised as below:

1. A closed-form analytical GFET model is derived. The distinct electron and hole mobilities are taken into account as well as the carrier density dependent mobility. Reasonable approximations are also proposed for the saturation velocity to eliminate the discontinuity in g_m caused by the two-region V_{sat} function. The transition of capacitance weighting factor from 0.5 to 1 is preserved with the proposed α function in Eq. (3.55) to improve the accuracy near Dirac point.

2. The feasibility of GFET NFC based on Linvill's technique is explored. Although the graphene mixers and amplifiers have been demonstrated experimentally, the NFC utilising GFETs as active elements has never been studied. With the developed GFET model, the Linvill's NFC utilising a pair of cross-couple GFET is simulated. The simulation results show that the circuit exhibits negative impedance at VHF frequency.

3. The NFC based on the NDR behaviour of GFET is explored. The potential of NDR phenomenon observed in GFET remains unexplored before. With the developed GFET model, the implementation of NDR to realise NFC is conducted. The simulation

results demonstrate negative impedance up to 2 GHz.

4. The bandwidth extension of HIS is demonstrated with NFCs achieved from NDR of GFET. A bandwidth improvement from 23% to 54.6% is achieved.

6.2 Future Work

Based on the work presented in this thesis, the following aspects are proposed as the potential further research:

1. **Temperature dependent carrier mobility.** The GFET model derived in this thesis assumes the device operates at room temperature. However, as shown in Fig. 3.8, the carrier mobility varies with the increase of temperature as well. Thus, it is necessary to include the temperature effects into the model so that the temperature analysis can be performed in the circuit simulation.

2. **Extend the GFET model from monolayer to multilayer device.** The GFET proposed in this thesis works for monolayer graphene devices only. As the multilayer graphene provides different electronic property such as a tunable bandgap in bilayer graphene, it is interesting to explore the extension of the model from monolayer to multilayer GFET.

3. **Explore the modelling of short-channel effects.** As the drift-diffusion transport theory is used in the proposed model, it is capable of simulating relatively long-channel devices only. For high frequency applications, it is necessary to scale the channel length of GFET, which unfortunately brings short-channel effects that are not modelled in this work. Hence, it is necessary to extend the model for short-channel devices.

4. **Experimental demonstration of graphene NFC.** The graphene NFCs are studied in this thesis through circuit simulations. As the performance of identical GFETs on the same die can differ from each other due to the immature fabrication process, it is

challenge to predict the performance of a graphene circuit even with an accurate GFET model. Therefore, it is interesting to explore the graphene NFC experimentally.

Appendix A

List of Publications

Journal Publications

1. **Jing Tian**, Deepak Singh Nagarkoti, Khalid Z Rajab, and Yang Hao. High impedance surface loaded with graphene non-Foster circuits for low-profile antennas. *IEEE Antennas and Wireless Propagation Letters*, 16:2655-2658, 2017

2. **Jing Tian**, Deepak Singh Nagarkoti, Khalid Z Rajab, and Yang Hao. Graphene-based tunable non-Foster circuit for VHF applications. *AIP Advances*, 6(6):065202, 2016

3. **Jing Tian**, Anestis Katsounaros, Darryl Smith, and Yang Hao. Graphene field-effect transistor model with improved carrier mobility analysis. *IEEE Transactions on Electron Devices*, 62(10):3433–3440, 2015

Conference Publications

1. **Jing Tian**, Deepak Singh Nagarkoti, Khalid Z Rajab, and Yang Hao. Negative impedance converter based on graphene field-effect transistor. In *Graphene Week, Warsaw, Poland.* Graphene Flagship, 2016

2. **Jing Tian**, Anestis Katsounaros, Darryl Smith, and Yang Hao. Accurate modelling of graphene field effect transistor for wireless communications. In *Antennas and Propagation (EuCAP), 2016 10th European Conference on*, pages 1–2. IEEE, 2016

3. **Jing Tian** and Yang Hao. Spice-like graphene field effect transistor model for active THz radiation and detection. In *IEEE International Symposium on Antenna and Propogation and North American Radio Sicence Meeting, Vancouver, BC, Canada.* Graphene Flagship, 19-24 July, 2015

Appendix B

Analytical Expressions

The analytical expression for the numerator integral of Eq. (3.8) is given by Eq. (B.1) as

$$
\begin{aligned}
\text{Intup} \;=\; & \frac{1}{2}dms \left[\frac{2h\left(2c^2m^2 - 3cm + 2\right)(bm - a)}{\sqrt{m}(cm - 1)^{3/2}} \tanh^{-1}\left(\frac{V_{ch}\sqrt{cm - 1}}{\sqrt{m}\sqrt{cV_{ch}^2 + 1}} \right) \right. \\
& + \; \frac{z\left(2c^2m^2 - 3cm + 2\right)(a - bm)}{(cm - 1)^2} \ln\left(m + V_{ch}^2\right) + \frac{z(b - ac)}{c(cm - 1)\left(cV_{ch}^2 + 1\right)} \\
& - \; \frac{z\left(ac^2m - 2bcm + b\right)}{c(cm - 1)^2} \ln\left(cV_{ch}^2 + 1\right) + 4\sqrt{c}h(a - bm)\sinh^{-1}\left(\sqrt{c}V_{ch}\right) \\
& + \; 2hV_{ch}\sqrt{cV_{ch}^2 + 1}\left(\frac{ac - b}{(cm - 1)\left(cV_{ch}^2 + 1\right)} + b \right) + 2bV_{ch}^2 z \Bigg] \\
& + \; mz\left[\frac{b\sqrt{cV_{ch}^2 + 1}}{c} + \frac{(a - bm)}{\sqrt{cm - 1}}\tan^{-1}\left(\frac{\sqrt{cV_{ch}^2 + 1}}{\sqrt{cm - 1}} \right) \right] \\
& + \; hm\left[\frac{(a - bm)}{\sqrt{m}}\tan^{-1}\left(\frac{V_{ch}}{\sqrt{m}} \right) + bV_{ch} \right] \\
& + \; qn_{pud}h\frac{m}{m + \left(\dfrac{V_{cs} + V_{cd}}{2}\right)^2}V_{ds}
\end{aligned}
\tag{B.1}
$$

165

The analytical expression for the denominator integral of Eq. (3.8) is is given by Eq. (B.2) as

$$
\begin{aligned}
\text{Intdown} \;=\; & mz\left[\frac{(fm-1)(bm-a)}{\sqrt{cm-1}(a-bm+n_{pud})(e-fgm+g)}\tan^{-1}\left(\frac{\sqrt{cV_{ch}^2+1}}{\sqrt{cm-1}}\right)\right.\\
& +\;\frac{\sqrt{b}\,n_{pud}(b-f(a+n_{pud}))}{\text{Deno}_1}\tan^{-1}\left(\frac{\sqrt{b}\sqrt{cV_{ch}^2+1}}{\sqrt{c(a+n_{pud})-b}}\right)\\
& +\left.\frac{e\sqrt{f}(afg-b(e+g))}{\text{Deno}_2}\tan^{-1}\left(\frac{\sqrt{f}\sqrt{g}\sqrt{cV_{ch}^2+1}}{\sqrt{c(e+g)-fg}}\right)\right]\\
& +\;dmsz\left[\frac{\text{Nume}_1}{\text{Deno}_3}\ln\left(a+bV_{ch}^2+n_{pud}\right)+\frac{\text{Nume}_2}{\text{Deno}_4}\ln\left(e+fgV_{ch}^2+g\right)\right.\\
& +\;\frac{\text{Nume}_3}{2(cm-1)^2(-ac+b-cn_{pud})^2(ce+cg-fg)^2}\ln\left(cV_{ch}^2+1\right)\\
& +\;\frac{\text{Nume}_4}{2(cm-1)^2(a-bm+n_{pud})(e-fgm+g)}\ln\left(m+V_{ch}^2\right)\\
& +\left.\frac{-ac^2+acf+bc-bf}{2(cm-1)\left(cV_{ch}^2+1\right)(ac-b+cn_{pud})(ce+cg-fg)}\right]\\
& +\;hm\left[\frac{\text{Nume}_5}{f^{3/2}g^{5/2}\sqrt{e+g}(e-fgm+g)}\tan^{-1}\left(\frac{\sqrt{f}\sqrt{g}V_{ch}}{\sqrt{e+g}}\right)\right.\\
& -\;\frac{(fm-1)\left(ds\left(2c^2m^2-3cm+2\right)+1\right)}{\sqrt{m}(e-fgm+g)}\tan^{-1}\left(\frac{V_{ch}}{\sqrt{m}}\right)\\
& -\left.\frac{cdsV_{ch}(2c(e+fgm)-3fg)}{fg^2}+\frac{2c^2dsV_{ch}^3}{3g}\right]
\end{aligned}
$$

(B.2)

$$
\begin{aligned}
\text{Nume}_1 \;=\; & -2a^3c^2fn_{pud}+2a^2bc^2n_{pud}+3a^2bcfn_{pud}-6a^2c^2fn_{pud}^2\\
& +\;2b^3n_{pud}-6ac^2fn_{pud}^3-3b^2cn_{pud}^2-2b^2fn_{pud}^2+2bc^2n_{pud}^3\\
& -\;2ab^2fn_{pud}+4abc^2n_{pud}^2-2c^2fn_{pud}^4+6abcfn_{pud}^2\\
& -\;3ab^2cn_{pud}+3bcfn_{pud}^3
\end{aligned}
$$

(B.3)

$$
\begin{aligned}
\text{Nume}_2 \;=\;& 2bc^2e^4 + 6bc^2e^3g - 3bce^3fg + 6bc^2e^2g^2 - 6bce^2fg^2 + 2be^2f^2g^2 \\
+\;& 2bef^2g^3 - 2ac^2efg^3 + 3acef^2g^3 + 3ace^2f^2g^2 - 2ac^2e^3fg \\
-\;& 3bcefg^3 + 2bc^2eg^3 - 2aef^3g^3 - 4ac^2e^2fg^2
\end{aligned}
\tag{B.4}
$$

$$
\begin{aligned}
\text{Nume}_3 \;=\;& 2abc^4gm - a^2c^5gm + 2b^2c^2fgm - 4abc^3fgm + 2a^2c^4fgm - b^2cf^2gm \\
+\;& 2abc^2ef - 4abc^3efm - b^2cef - ac^3f^2gmn_{pud} + 2abc^4em - a^2c^5em \\
+\;& 2b^2c^2efm + 2bc^2efn_{pud} + 2abc^2f^2gm - a^2c^3ef + 2bc^4emn_{pud} \\
+\;& 2a^2c^4efm - ac^3efn_{pud} - bc^3gn_{pud} + 2bc^2fgn_{pud} - bcf^2gn_{pud} \\
+\;& 2ac^4efmn_{pud} + 2bc^4gmn_{pud} - ac^5gmn_{pud} - 4bc^3fgmn_{pud} \\
-\;& a^2c^3f^2gm - b^2c^3em - b^2c^3gm - bc^3en_{pud} - 3bc^3efmn_{pud} \\
+\;& 2ac^4fgmn_{pud} + 2bc^2f^2gmn_{pud} - ac^5emn_{pud}
\end{aligned}
\tag{B.5}
$$

$$
\begin{aligned}
\text{Nume}_4 \;=\;& 2bfm^2 + 2ac^2m^2 + 3acfm^2 - 3acm - 2afm + 2bc^2fm^4 \\
+\;& 2a - 2ac^2fm^3 - 2bc^2m^3 - 3bcfm^3 - 2bm + 3bcm^2
\end{aligned}
\tag{B.6}
$$

$$
\text{Nume}_5 = e\left(2c^2ds(e+g)^2 - 3cdfgs(e+g) + f^2g^2(2ds+1)\right)
\tag{B.7}
$$

$$
\text{Deno}_1 = \sqrt{c(a+n_{pud}) - b(a - bm + n_{pud})(b(e+g) - fg(a+n_{pud}))}
\tag{B.8}
$$

$$\text{Deno}_2 = \sqrt{g}\sqrt{c(e+g) - fg}(e - fgm + g)(fg(a + n_{pud}) - b(e+g)) \tag{B.9}$$

$$\text{Deno}_3 = 2(ac - b + cn_{pud})^2(a - bm + n_{pud})(-afg + be + bg - fgn_{pud}) \tag{B.10}$$

$$\text{Deno}_4 = 2g(ce + cg - fg)^2(e - fgm + g)(-afg + be + bg - fgn_{pud}) \tag{B.11}$$

Appendix C

Capacitance Model

$$C_{gg} = \frac{\partial Q_g}{\partial V_{cd}} \times \frac{\partial V_{cd}}{\partial V_g} + \frac{\partial Q_g}{\partial V_{cs}} \times \frac{\partial V_{cs}}{\partial V_g}, \tag{C.1}$$

$$C_{gd} = -\frac{\partial Q_g}{\partial V_{cd}} \times \frac{\partial V_{cd}}{\partial V_d} \tag{C.2}$$

$$C_{dd} = \frac{\partial Q_d}{\partial V_{cd}} \times \frac{\partial V_{cd}}{\partial V_d} \tag{C.3}$$

$$C_{dg} = -\frac{\partial Q_d}{\partial V_{cd}} \times \frac{\partial V_{cd}}{\partial V_g} - \frac{\partial Q_d}{\partial V_{cs}} \times \frac{\partial V_{cs}}{\partial V_g}, \tag{C.4}$$

$$C_{ds} = C_{dd} - C_{dg} \tag{C.5}$$

$$C_{gs} = C_{gg} - C_{gd} \tag{C.6}$$

$$\frac{\partial Q_g}{\partial V_{cd}} = \frac{k_c W L_{eff}}{2} \left(\frac{-g'(V_{cd}) [f(V_{ch})]_{V_{cs}}^{V_{cd}}}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^2} + \frac{h(V_{cd})}{[g(V_{ch})]_{V_{cs}}^{V_{cd}}} \right) \tag{C.7}$$

$$\frac{\partial Q_g}{\partial V_{cs}} = \frac{k_c W L_{eff}}{2} \left(\frac{g'(V_{cs}) [f(V_{ch})]_{V_{cs}}^{V_{cd}}}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^2} - \frac{h(V_{cs})}{[g(V_{ch})]_{V_{cs}}^{V_{cd}}} \right) \tag{C.8}$$

$$
\begin{aligned}
\frac{\partial Q_d}{\partial V_{cd}} = \ & -\frac{k_c W L_{eff}^2}{2L} \left(\frac{-2g'(V_{cd})}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^3} \left(g(V_{cs}) [f(V_{ch})]_{V_{cs}}^{V_{cd}} \right) + [m(V_{ch})]_{V_{cs}}^{V_{cd}} \right. \\
& + \left. \frac{1}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^2} (g(V_{cs}) h(V_{cd}) + n(V_{cd})) \right)
\end{aligned} \tag{C.9}
$$

$$
\begin{aligned}
\frac{\partial Q_d}{\partial V_{cs}} = \ & -\frac{k_c W L_{eff}^2}{2L} \left(\frac{2g'(V_{cs})}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^3} \left(g(V_{cs}) [f(V_{ch})]_{V_{cs}}^{V_{cd}} + [m(V_{ch})]_{V_{cs}}^{V_{cd}} \right) \right. \\
& + \left. \frac{1}{\left([g(V_{ch})]_{V_{cs}}^{V_{cd}} \right)^2} \left(g'(V_{cs}) [f(V_{ch})]_{V_{cs}}^{V_{cd}} - g(V_{cs}) h(V_{cs}) - n(V_{cs}) \right) \right)
\end{aligned} \tag{C.10}
$$

$$\frac{\partial V_{cd}}{\partial V_g} = -\frac{\partial V_{cd}}{\partial V_d} = \left(1 + \mathrm{sgn}(V_{cd}) \frac{k_c V_{cd}}{C_t + C_b} \right)^{-1} ; \tag{C.11}$$

$$\frac{\partial V_{cd}}{\partial V_g} = \left(1 + \mathrm{sgn}(V_{cs}) \frac{k_c V_{cs}}{C_t + C_b} \right)^{-1} ; \tag{C.12}$$

$$g(V_{ch}) = \frac{-V_{ch}^3}{3} - \mathrm{sgn}(V_{ch}) \frac{k_c V_{ch}^4}{4(C_t + C_b)} \tag{C.13}$$

$$g^{'}\left(V_{ch}\right) = -V_{ch}^2 - \text{sgn}\left(V_{ch}\right) \frac{k_c V_{ch}^3}{C_t + C_b} \tag{C.14}$$

$$h\left(V_{ch}\right) = \text{sgn}\left(V_{ch}\right) V_{ch}^4 + \frac{k_c V_{ch}^5}{C_t + C_b} \tag{C.15}$$

$$n\left(V_{ch}\right) = \text{sgn}\left(V_{ch}\right) \frac{V_{ch}^7}{3} + \frac{7 k_c V_{ch}^8}{12\left(C_t + C_b\right)} + \text{sgn}\left(V_{ch}\right) \frac{k_c^2 V_{ch}^9}{4\left(C_t + C_b\right)^2} \tag{C.16}$$

$$f\left(V_{ch}\right) = \text{sgn}\left(V_{ch}\right) \frac{V_{ch}^5}{5} + \frac{k_c V_{ch}^6}{6\left(C_t + C_b\right)} \tag{C.17}$$

$$m\left(V_{ch}\right) = \text{sgn}\left(V_{ch}\right) \frac{V_{ch}^8}{24} + \frac{7 k_c V_{ch}^9}{108\left(C_t + C_b\right)} + \text{sgn}\left(V_{ch}\right) \frac{k_c^2 V_{ch}^{10}}{40\left(C_t + C_b\right)^2} \tag{C.18}$$

where $k_c = (2q^2/\pi)(q/(\hbar v_F)^2)$ and $L_{eff} = L + \mu \mid V_{ds} \mid /v_F$.